Codes description

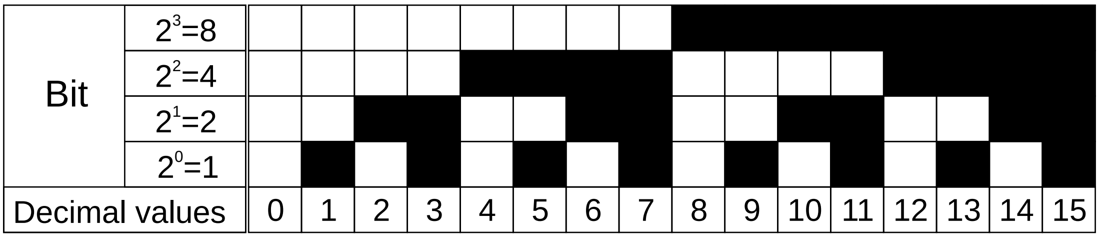
TEKEL INSTRUMENTS

CODES CHARACTERISED BY SEVERAL CHANGES A STEP

1) BINARY NATURAL CODE

The Binary Natural code is characterised by two switching levels: TRANSPARENT/DARK, OFF/ON, 0/1, etc.
The code is generally represented by a “1” or a “0”. The graphic representations of “1” and “0” are called “Bit”, and are directly related to binary arithmetics.
Every value can be represented with a sequence of several Bit from “1” or from “0”. Each Bit of the binary sequence has a fixed position value: from 2^{0} to 2^{n}. This value is equal to 2 raised to the power indicated by the position itself (Fig. 1).

BINARY NATURAL CODE



Example of factorisation of the Decimal number “11”.
$1 x 2^{3} + 0 x 2^{2} + 1 x 2^{1} + 1 x 2^{0} =$
$8 + 0 + 2 + 1 = 11$
Every digit can be represented adding further bit up to 2^{n}”

Fig. 1

2) BCD CODE (8-4-2-1)

Converting a decimal number into a binary value and vice versa is a very complex operation. The BCD or 8-4-2-1 code allows the direct coding of the single digits of the decimal numeration (Fig.2). Devices such as counters, position displays, etc, operate according to this code.

BCD CODE (o 8 - 4 - 2 - 1)

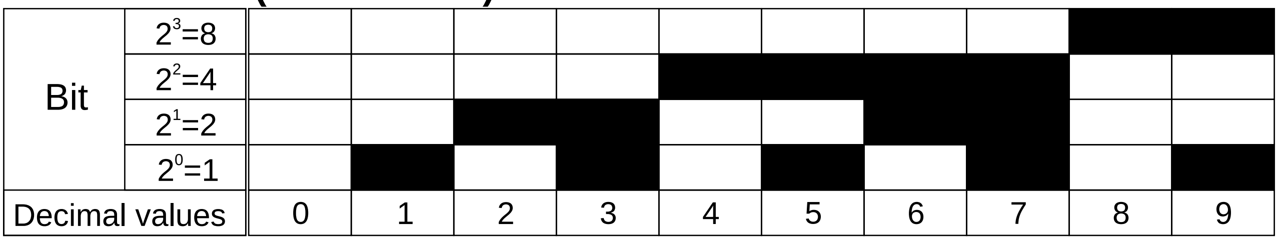


Fig. 2

Several Bit can change simultaneously with the a.m. codes. This can be observed for example when passing from value 7 to value 8 (Fig. 1-2). If switching is not carried out at exactly the same time, some errors in evaluation may arise.
AMBIGUITY is an inherent error in encoder caused by the fact that two “on/off” measuring devices cannot generate and therefore transfer states at precisely the identical instant each and every time. In order to avoid this problem, different codes with a single change per step can be used.
Examples of codes such as these are GRAY and GRAY EXCESS 3 than can be used respectively as options for the BINARY CODE and the BCD CODE. Fig.3 shows the ambiguity errors that can be found in codes different from GRAY. To avoid these errors TEKEL's absolute encoders read pattern in GRAY code or similar (see Fig. 4): the “memories” automatically change the states with the appropriate code.

POSITION	GRAY 2^4 2^3 2^2 2^1 2^0	BINARY	BCD
0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0
1	0 0 0 0 1	0 0 0 0 1	0 0 0 0 1
2	0 0 0 1 1	0 0 0 1 0	0 0 0 1 0
3	0 0 0 1 0	0 0 0 1 1	0 0 0 1 1
4	0 0 1 1 0	0 0 1 0 0	0 0 1 0 0
5	0 0 1 1 1	0 0 1 0 1	0 0 1 0 1
6	0 0 1 0 1	0 0 1 1 0	0 0 1 1 0
7	0 0 1 0 0	0 0 1 1 1	0 0 1 1 1
8	0 1 1 0 0	0 1 0 0 0	0 1 0 0 0
9	0 1 1 0 1	0 1 0 0 1	0 1 0 0 1
10	0 1 1 1 1	0 1 0 1 0	1 0 0 0 0
11	0 1 1 1 0	0 1 0 1 1	1 0 0 0 1
12	0 1 0 1 0	0 1 1 0 0	1 0 0 1 0

Fig. 3

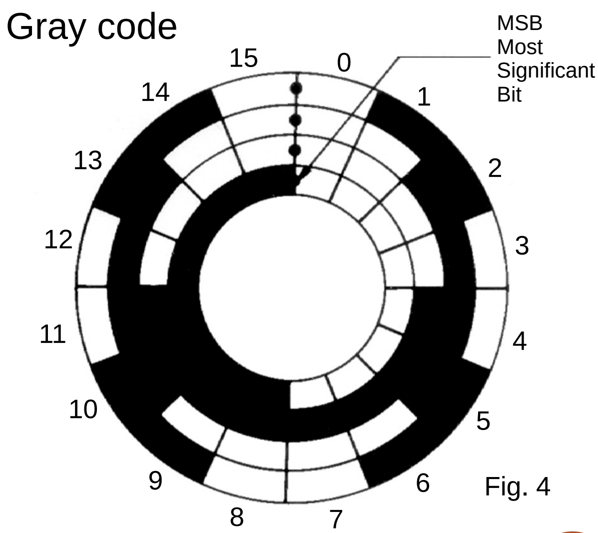


Fig. 4

CODES CHARACTERIZED BY A SINGLE CHANGE A STEP

1) GRAY CODE

It has the advantage of being monostropic, since it requires only a single bit (channel, disc path, etc.) to change when passing from any number to an adjacent number, from TRANSPARENT to DARK, from OFF to ON, from 0 to 1, or vice versa.
If the transparent/dark edge of each path (Bit) is not well defined or if the readout is not perfectly true, small angular errors may arise but, in this case, there will be absolutely no evaluation errors.
The GRAY code is also called "reflected code". Fig. 5 shows that the second part of the number 8 15 has the same sequence of the number 0 7, but reflected. The only exception is the Bit number 4 (Bit most significant or MSB) that separates exactly the code into two parts. Due to these characteristics, the GRAY code can be used only for numbers of EVEN value.

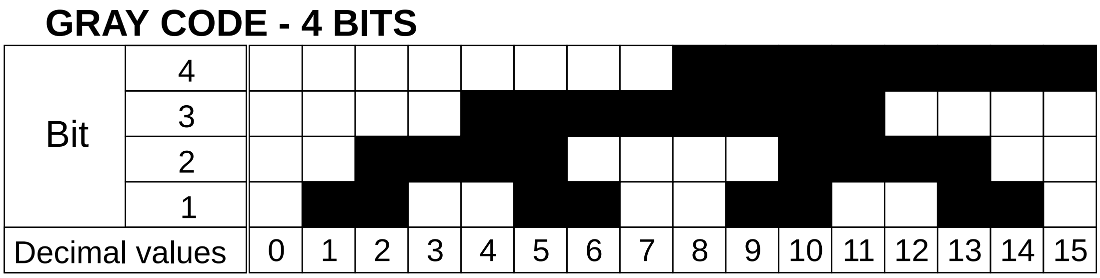


Fig. 5

Particular characteristics of a reflected code
It is possible to change the counting by inverting the most significant Bit (see Fig. 5, Bit 4). This way it is possible to establish if the Gray code must increase in case of CW rotation and decrease in case of CCW rotation.

2) GRAY CODE SIMMETRICALLY CUT OTHERWISE CALLED GRAY EXCESS…

This code allows the translation of a non-binary value onto disc without renouncing to any of the single switching features. New values are assigned to Bits sequences for converting them from Gray to BCD, from Gray to Binary, etc. The decimal value is corrected with a "K" value (Excess…). Example: the value "K" is calculated as follows:
n= number of bits necessary to represent in Binary the maximum wished value of division;
p= number of division or steps (0 19 = 20)

$$K = \frac{2^n - P}{2} = \frac{2^5 - 20}{2} = \frac{32 - 20}{2} = 6 = \text{GRAY ECCESSO 6}$$

So, the zero value will be the number 6 in Gray code.
This is the most common method for calculating code for encoders with divisions on 360° or any other even value

3)GRAY CODE CENTRALLY CUT ><

The difference is that the part to be cut is the central part of the code. Therefore, for any number of divisions, the code of the first division will be always zero and will be immediately identified (Fig. 6). The paert to be cut is identifiable with a similar criteria as previous one: example $K = 2^n - P = 2^5 - 20 = 12$.
Cut start = 20/2 = 10 that means: 12 bit are cut starting from the bit 10 and up to the bit 21 included.

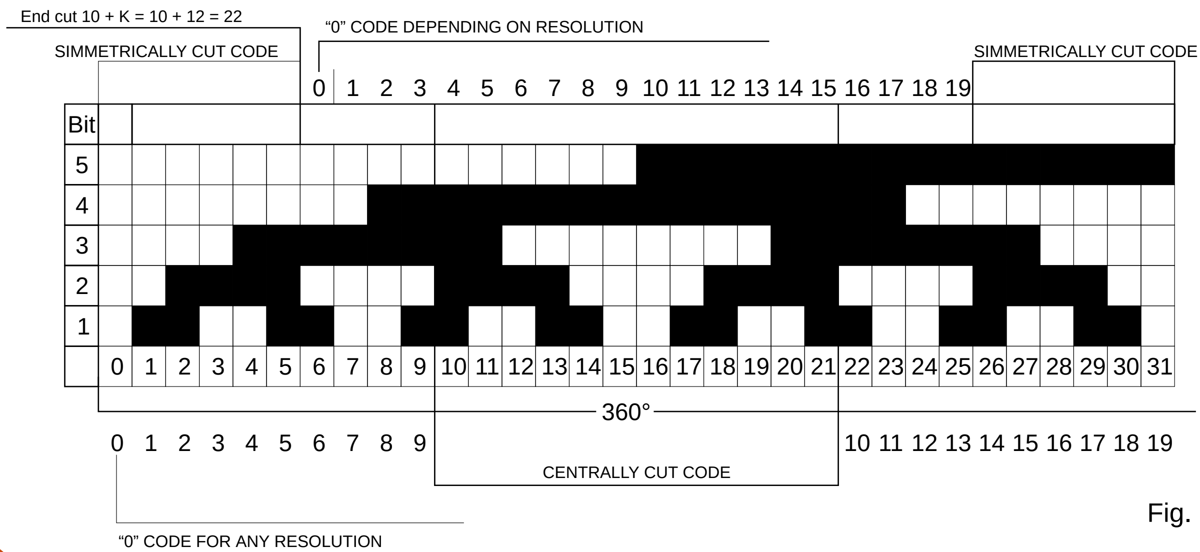
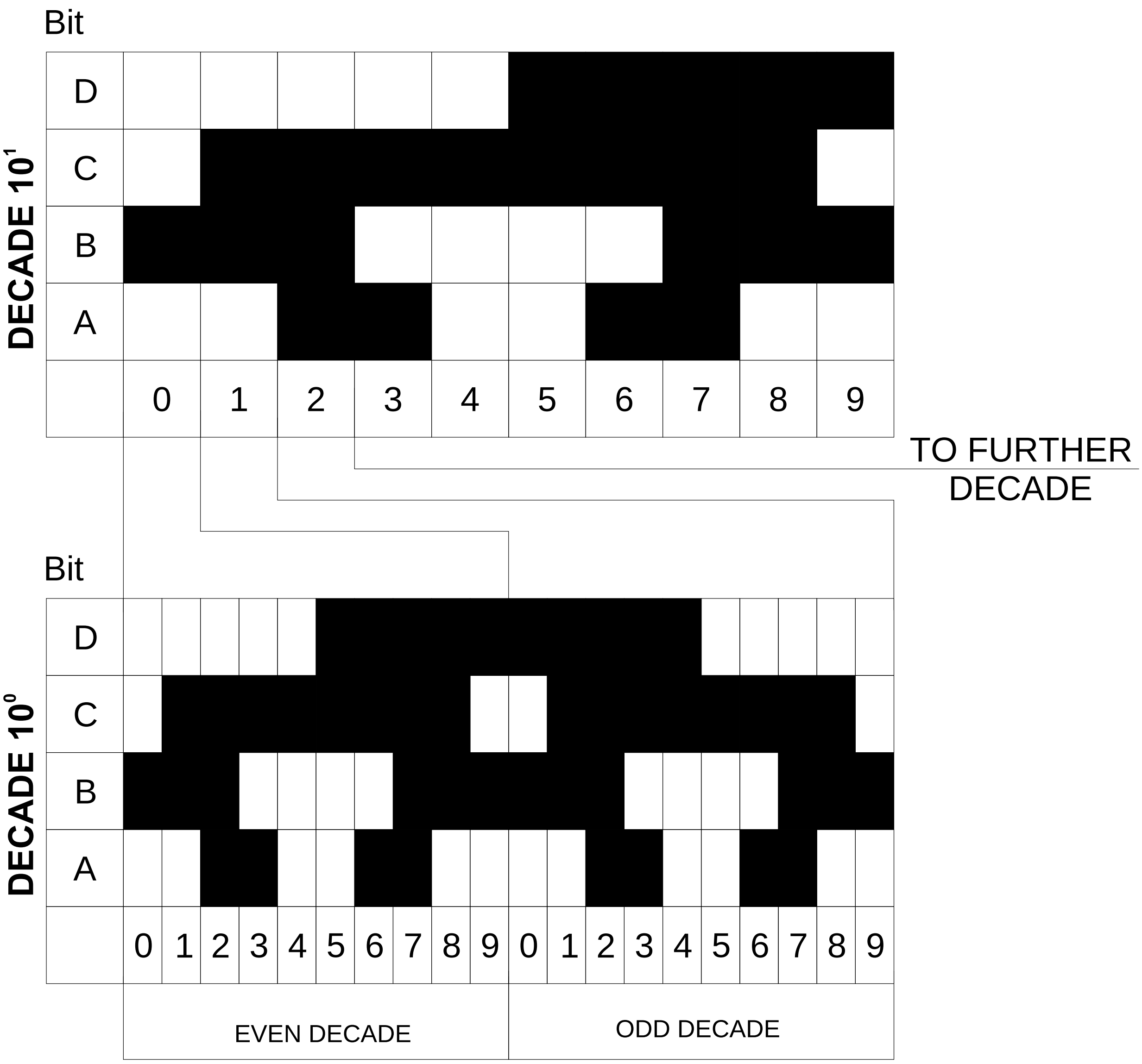


Fig. 6

4) GRAY CODE EXC 3

It is a decimal code that follows the a.m. rule of code Gray Excess..
As in BCD code, the digits are coded from 0 to 9, therefore 4 Bits are necessary to constitute each decimal digit.
The code structure is: a single change per step and, like the Gray code, it cannot be directly evaluated.

GRAY CODE EXC 3
FOR 100 DIVISION (0÷99)



The sequence is repeated for 5 times
(20÷29; 30÷39; 40÷49; 50÷59; ect.)

Fig. 7

CODES EXAMPLE: Natural binary BCD Gray Excess 3

Decimal number	GRAY CODE (4 3 2 1 0)	BINARY CODE (32 16 8 4 2 1)	BCD CODE 2° decade (8 4 2 1)	BCD CODE 1° decade (8 4 2 1)	GRAY EXC 3 CODE 2° decade (3 2 1 0)	GRAY EXC 3 CODE 1° decade (3 2 1 0)
0	0 0 0 0 0	0 0 0 0 0 0	0 0 0 0	0 0 0 0	0 0 1 0	0 0 1 0
1	0 0 0 0 1	0 0 0 0 0 1	0 0 0 0	0 0 0 1	0 0 1 0	0 1 1 0
2	0 0 0 1 1	0 0 0 0 1 0	0 0 0 0	0 0 1 0	0 0 1 0	0 1 0 0
3	0 0 0 1 0	0 0 0 0 1 1	0 0 0 0	0 0 1 1	0 0 1 0	0 1 0 1
4	0 0 1 1 0	0 0 0 1 0 0	0 0 0 0	0 1 0 0	0 0 1 0	1 1 0 1
5	0 0 1 1 1	0 0 0 1 0 1	0 0 0 0	0 1 0 1	0 0 1 0	1 1 0 0
6	0 0 1 0 1	0 0 0 1 1 0	0 0 0 0	0 1 1 0	0 0 1 0	1 1 0 1
7	0 0 1 0 0	0 0 0 1 1 1	0 0 0 0	0 1 1 1	0 0 1 0	1 1 1 1
8	0 1 1 0 0	0 0 1 0 0 0	0 0 0 0	1 0 0 0	0 0 1 0	1 1 1 0
9	0 1 1 0 1	0 0 1 0 0 1	0 0 0 0	1 0 0 1	0 0 1 0	1 0 1 0
10	0 1 1 1 1	0 0 1 0 1 0	0 0 0 1	0 0 0 0	0 1 1 0	1 0 1 0
11	0 1 1 1 0	0 0 1 0 1 1	0 0 0 1	0 0 0 1	0 1 1 0	1 1 1 0
12	0 1 0 1 0	0 0 1 1 0 0	0 0 0 1	0 0 1 0	0 1 1 0	1 1 1 1
13	0 1 0 1 1	0 0 1 1 0 1	0 0 0 1	0 0 1 1	0 1 1 0	1 1 0 1
14	0 1 0 0 1	0 0 1 1 1 0	0 0 0 1	0 1 0 0	0 1 1 0	1 1 0 0
15	0 1 0 0 0	0 0 1 1 1 1	0 0 0 1	0 1 0 1	0 1 1 0	0 1 0 0
16	1 1 0 0 0	0 1 0 0 0 0	0 0 0 1	0 1 1 0	0 1 1 0	0 1 0 1
17	1 1 0 0 1	0 1 0 0 0 1	0 0 0 1	0 1 1 1	0 1 1 0	0 1 1 1
18	1 1 0 1 1	0 1 0 0 1 0	0 0 0 1	1 0 0 0	0 1 1 0	0 1 1 0
19	1 1 0 1 0	0 1 0 0 1 1	0 0 0 1	1 0 0 1	0 1 1 0	0 0 1 0
20	1 1 1 1 0	0 1 0 1 0 0	0 0 1 0	0 0 0 0	0 1 1 1	0 0 1 0

Fig. 8

ABSOLUTE ENCODERS are divided in two major groups:
SINGLE TURN: absolute encoders with a capacity equal to the resolution (i.e. 2048)
MULTI TURN: absolute encoders with a capacity equal to the single turn resolution multiplied by the number of turns (i.e. 8192x 4096)

TYPICAL APPLICATIONS

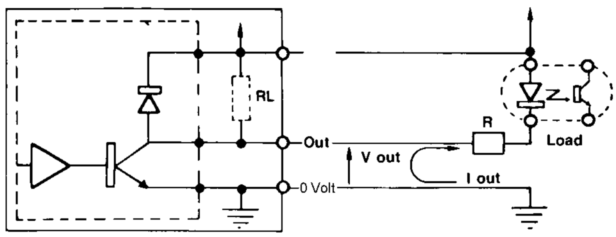
- Turrets positioning
- Plotter axis X-Y-Z positioning
- Rotary tables positioning
- Level measurements
- Length measurements for wood and metal processing
- Printing machines synchronism
- Radar antennas positioning
- Telescopes positioning
- Industrial robotics
- Timing and pressing machines control
- Speed control
- Numerically-controlled machine tools
- Crane control and positioning
- Cylinder memory control
- Automating computing scales
- Electronic cams and valves
- Nuclear-hydraulic power plants control
- Production and assembling lines (ex. car industry)

GENERAL CONVENTIONS

- Code and sense of rotation
  The value of code increases with CW of shaft as viewed from encoder shaft end.

- Logic
  positive logic (or code):
  Logic “1” = “HIGH” output voltage level
  Logic “0” = “LOW” output voltage level
  negative logic (or code)
  Logic “1” = “LOW” output voltage level
  Logic “0” = “HIGH” output voltage level

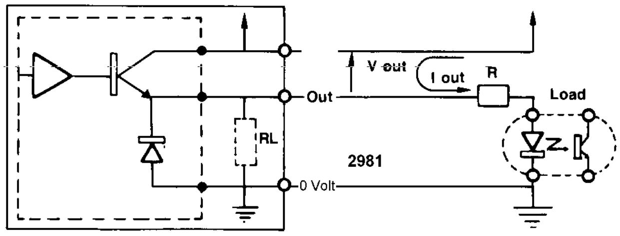
NPN (NEGATIVE LOGIC)



Order code
22 NPN open collector
23 NPN con pull-up internal

I out (SINK) 100 mA max
V out LOW 1,1 V max (a 100 mA)
HIGH Vcc (with pull-up resistor)
Pull-up resistor (RL) 5 Vcc RL = 680 Ohm
11÷30 Vcc RL = 4K7 Ohm

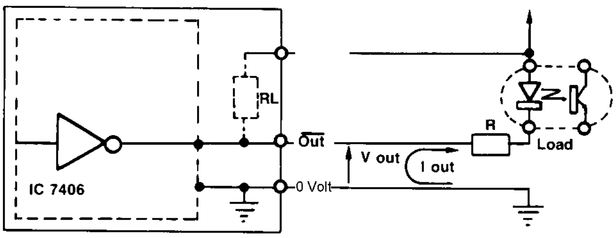
PNP (POSITIVE LOGIC)



Order code
20 PNP open collector
21 PNP con pull-down internal

***I out** (SOURCE) 100 mA max
V out HIGH Vcc -1,8 V min (a 100 mA)
LOW 0,2 V max (with pull-up resistor)
Pull-down resistor (RL) 5 Vcc RL = 680 Ohm
11÷30 Vcc RL = 4K7 Ohm

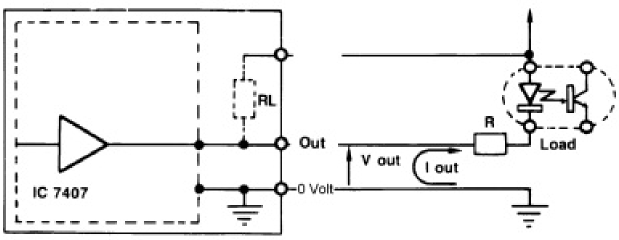
NPN - 7406 (NEGATIVE LOGIC)



Order code
10 NPN open collector
11 NPN con pull-up internal

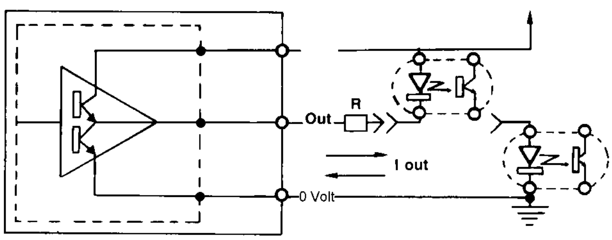
I out (SINK) 40 mA max
V out HIGH Vcc (with pull-up resistor)
LOW 0,7 V max (a 40 mA)
Pull-up resistor (RL) 5 Vcc RL = 680 Ohm
11÷30 Vcc RL = 4K7 Ohm

NPN - 7407 (POSITIVE LOGIC)



Order code
12 NPN open collector
13 NPN with internal pull-up

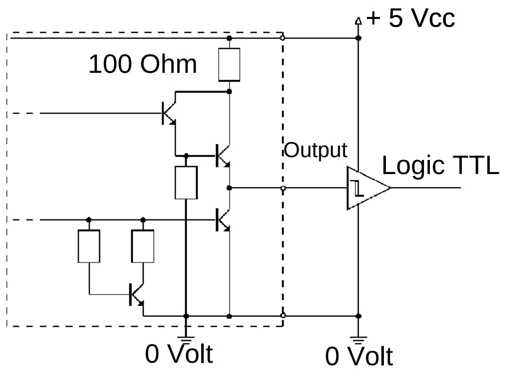
PUSH-PULL (POSITIVE LOGIC)



Order code **30**

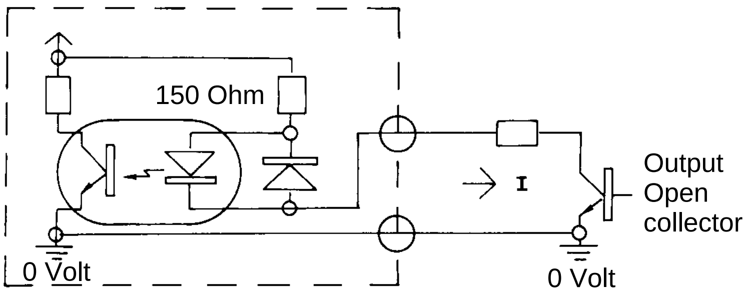
	5 Vcc PP
	11÷30 Vcc
I out (SINK o SOURCE)	15 mA max
V out HIGH=	Vcc -1V (a 15 mA)
LOW=	1V max (a 15 mA)

TTL OUTPUTS Ordering code 00, 01, 02, 03



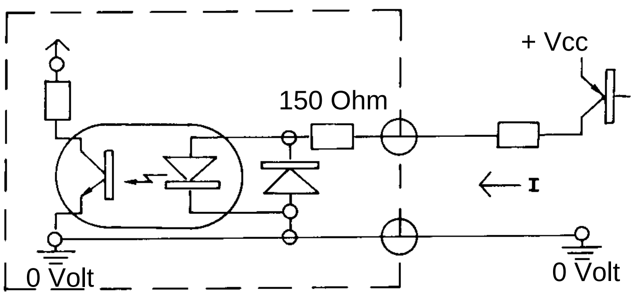
V Low (a 12 mA) = 0,25÷0,5 V
V High (a 12 mA) = 2,4÷3,1 V
I max = 2,5 mA

NPN INPUT - Ordering code L - U - M - T



I max =15 mA
I min = 6 mA
V max = 50 Vcc

PNP INPUT Ordering code P - W - C - X - N



I max = 15 mA
I min = 6 mA
V max = 50 Vcc

Description

The absolute encoder equipped with an analogical interface is usually connected to devices (PLC) provided with an analogical A/D/C converter. The connection occurs by means of a screened cable with a maximum of 8 conductors divided as follows: 2 conductors for the analogical signal (+L, -L), 2 conductors for power, 1 conductor for the up/down selection, 3 conductors for optional signals (STROBE, ZERO and CASE).
The analogical interface works with GRAY coded discs. This is then converted in a 10 Bits BINARY code by static logic circuits and then sent to a DAC.
The output analogical signal of the converter is then amplified to obtain from the interface a modulated current or voltage signal.
The current modulation version (4÷20 mA) has the function of controlling current in a line whose total resistance is generally 250 Ohm. The modulation occurs in such a way that, with the encoder set to zero code, on the line there is a current of 4 mA. This will gradually increase to reach 20 mA when the encoder will be in position 1023 code. The current increase is of 0.0156 mA for each encoder displacement step.
The voltage modulation versions behave similarly to the 4÷20 mA version: when the encoder is in zero position the output voltage on the line will be 1 Volt, 0 Volt, - 5 Volt or 10 Volt; it will reach the values of 5 Volt, 10 Volt, 10 Volt, +5 Volt or +10 Volt when the encoder will be in 1023 position. The above mentioned values correspond to the single characteristics of the analogical interface versions 1÷5 Volt, 0÷10 Volt, 5 Volt and 10 Volt. Unlike the 4÷20 mA version, the line employed with this version will have a very high total resistance so to avoid a voltage drop which would alter the actual value of the signal. In Fig. 28 and 29 the connections for the different voltages are shown. Particular attention must be paid to the connections of the cables' screens both for applications with PLC power supply and for encoders with a separate power supply.

EXAMPLE OF APPLICATION

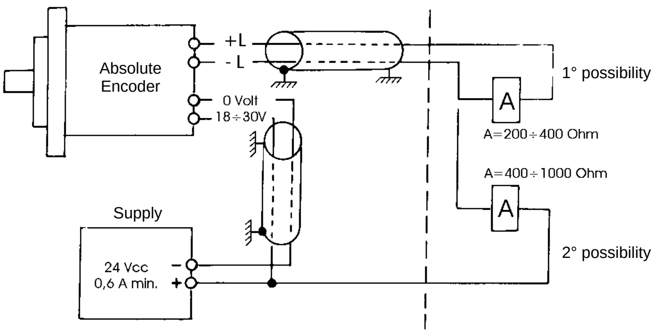


Fig. 9

SOURCE TYPICAL CONNECTION (4 ÷ 20 mA)

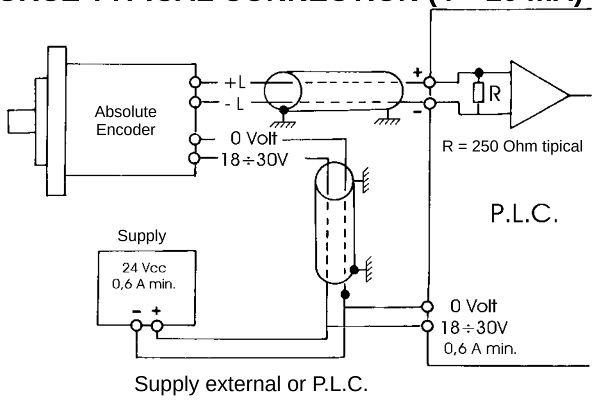


Fig. 10

VOLTAGE SOURCE

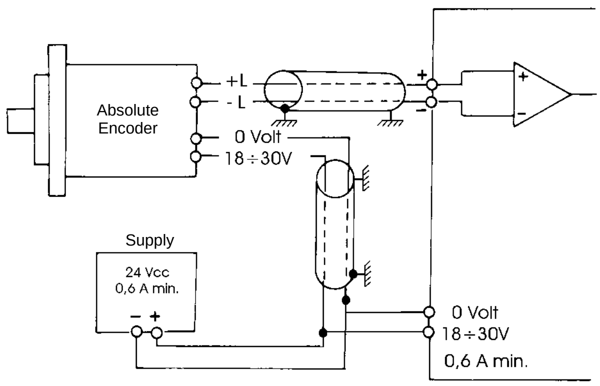


Fig. 11

RESOLUTIONS

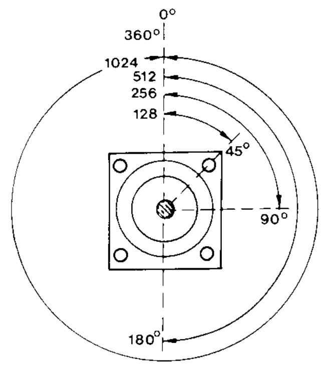
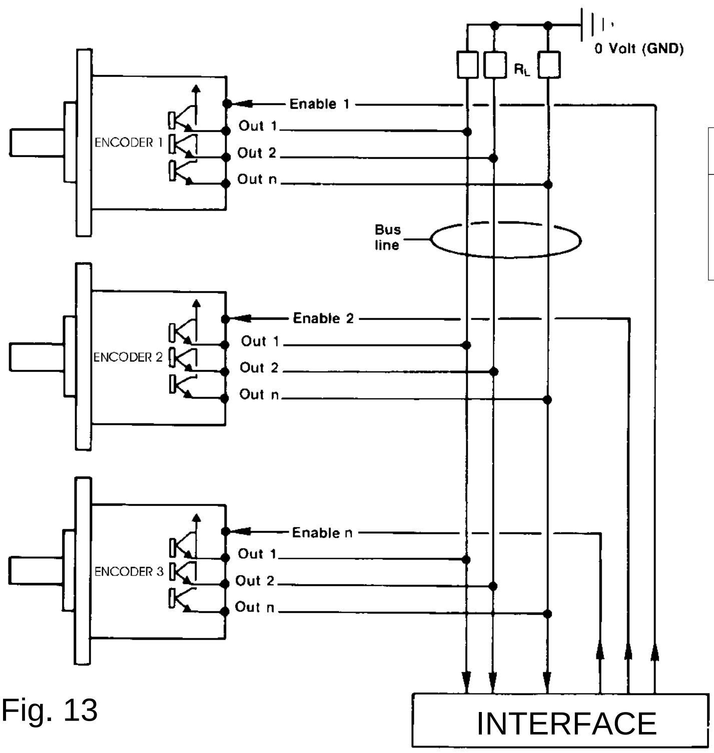


Fig. 12

STATE BUS TTL COMPATIBLE
Ordering code 41 (operating voltage 5 Vdc 5% or 11 ÷ 30 Vdc)

It is similar to BUS 3-STATE and NPN MULTIPLEXER version with the difference that the outputs are 100 mA open collector (positive logic) without pull-down resistor.
Each BUS line must end with a pull-down resistor linked up to 0 Volt (GND) (see Fig. 13).
To read the selected encoder a "LOW" signal may be addressed on pin 3-STATE: operating in this way the output transistors are set to "on" (Fig. 14). If on pin 3-STATE the signal "HIGH" appears the encoders are not operative.



Vcc (V)	R_L typical
5 11÷30	680 Ohm 4K7 Ohm

Fig. 13

Switch-over characteristics
T (enable) > 10 µs
t_{off} = 5 µs max
Electrical characteristics
INPUT PIN ENABLE
$V_{I\,LOW}$ = 0,7 V max
$V_{I\,HIGH}$ = Vcc max (5 - 11÷30) depending on input voltage power
$I_{I\,HIGH}$ > 1 mA min

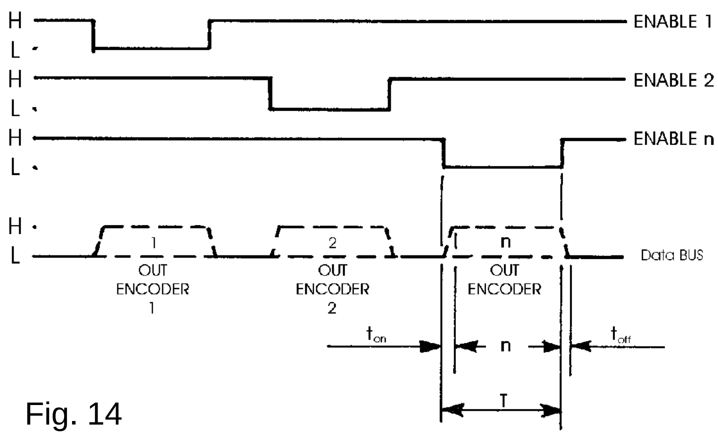


Fig. 14

NPN MULTIPLEXER
Order code 40 (operating voltage 5 Vdc 5% or 11 ÷ 30 Vdc)

NPN MULTIPLEXER option operates as above mentioned for the option BUS-3-STATE, with the difference that the outputs are 22, or 23 NPN 100 mA Open-Collector version (without pull-up resistor) and each BUS line must end with a pull-up resistor linked up to + Vdc. To read the selected encoder a “LOW” signal may be addressed to pin 3-STATE: in this way the transistor outputs are qualified to go “on” and “0 Volt”flows on the interested lines to form a code of the discrete shaft position (see Figs. 15 and 16). The transistors of the encoders not qualified in reading stay in “off” conditions to avoid interference with the encoder selected operative.

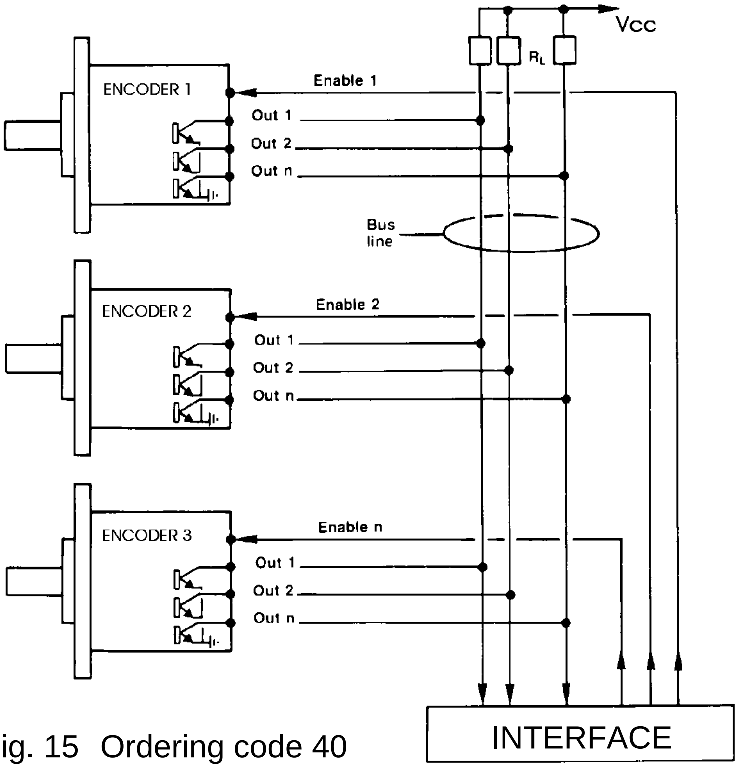


Fig. 15 Ordering code 40

Vcc (V)	R_L typical
5	680 Ohm
11÷30	4K7 Ohm

Electrical characteristics INPUT PIN (ENABLE)

$V_{I\,LOW}$ = 0,7 V max
$V_{I\,HIGH}$ = Vcc max (5 -11÷30) depending on input voltage power
$I_{I\,HIGH}$ > 1mA

Switch-over characteristics
T (enable) > 10 µs min
t_{ON} = 3 µs max
t_{OFF} = 5 µs max

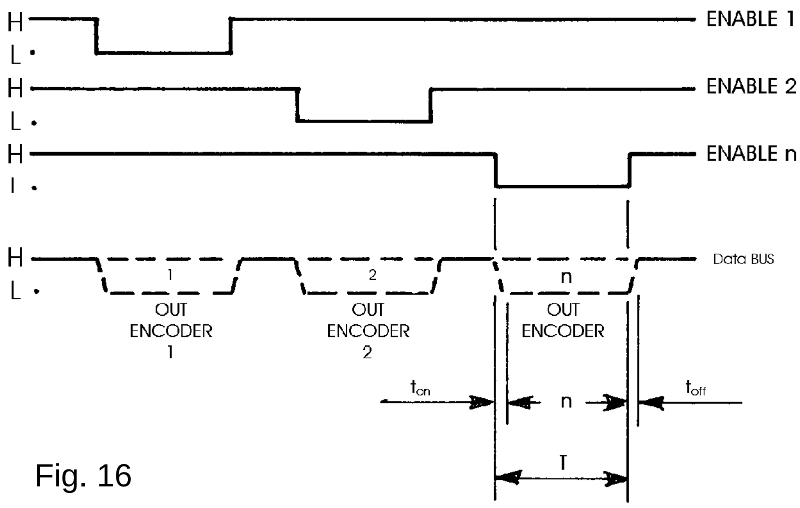


Fig. 16

ENABLE(3-STATE BUS TTL COMPATIBLE)
Ordering code 02 and 03 (operating voltage 5 Vdc only)

The 3-State function allows to connect some encoders in parallel to a unique input. Consequently the wire becomes simple and less expensive; however, only one encoder can be read at a time (Fig. 17). To read the selected encoder, a “LOW” signal may be addressed to pin 3-State; operating in this way outputs are qualified “HIGH” and “LOW” to form a code of the discrete shaft position. Of course the code will be automatically reset if the shaft is rotating and the input 3-State stays low. The encoders is not operative, because their inputs 3-State are “HIGH” persist in state of high impedance (Fig.17).
The output signals of one encoder will not change over simultaneously with the control “ENABLE” (on pin 3-STATE) but its responses are delayed; for this reason it is convenient to delay the reading of the data, or the reading of another encoder (see Fig. 18). As example, the Fig. 18 shows the connection between the ENABLE 1, 2 and 3 and the corresponding output signals.

TKC 3-state option
Electrical characteristics (TTL compatible))

INPUT
$V_{I\ LOW}$ =0,8 V max
$V_{I\ HIGH}$ =2 V min
$I_{I\ LOW}$ =-0,4 mA
$I_{I\ HIGH}$ =20 µA

OUTPUT
$V_{O\ LOW}$ = 0,5 V max
$V_{O\ HIGH}$ = 2,4 V min
$I_{O\ LOW}$ = 24 mA max
$I_{O\ HIGH}$ = -2,6 mA max
$I_{O\ OFF}$ = 20 µA max

GND = 0 V
Vcc$_{MIN}$ = 4,75 V
Vcc$_{MAX}$ = 5,25 V

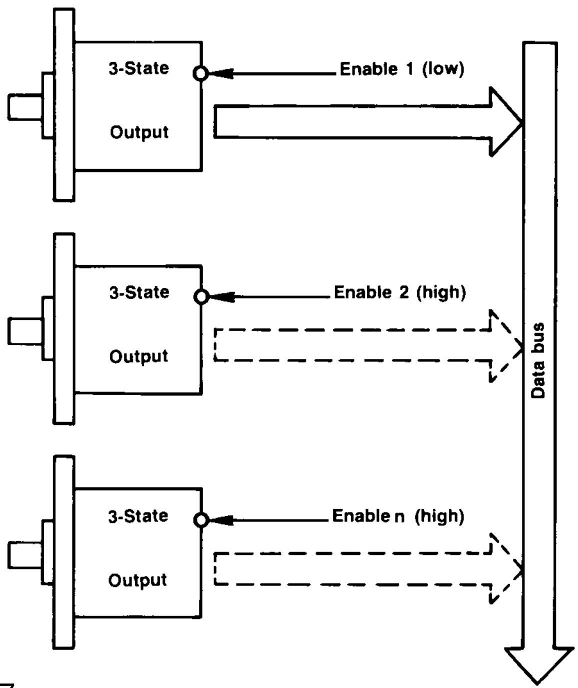


Fig. 17 Order code 02, 03

Switching characteristics (ENABLE)

T = 4 µs min
t_{on} = 0,5 µs max
t_{off} = 0,5 µs max

N.B. The specified times are valid for Encoder-Bus connections with a length inferior or equal to 1 meter and a maximum of five connected encoders or for a total cable length of 5 meters. For longer cables, the times may be subjected to modifications.

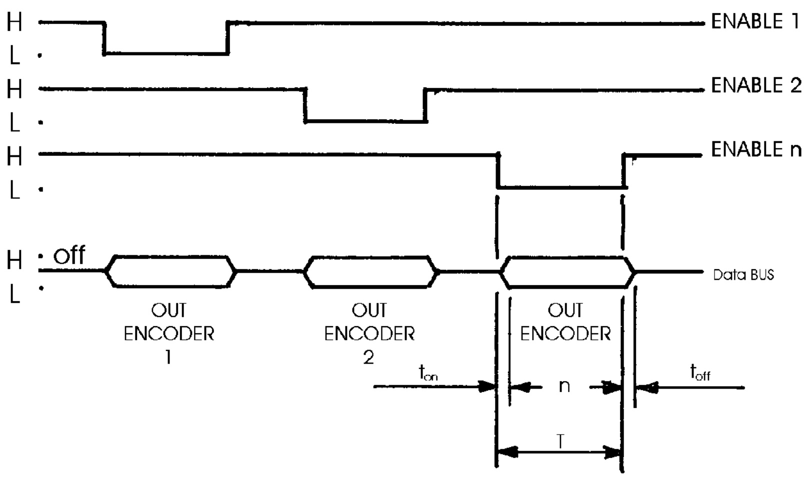


Fig. 18

GENERAL CHARACTERISTICS

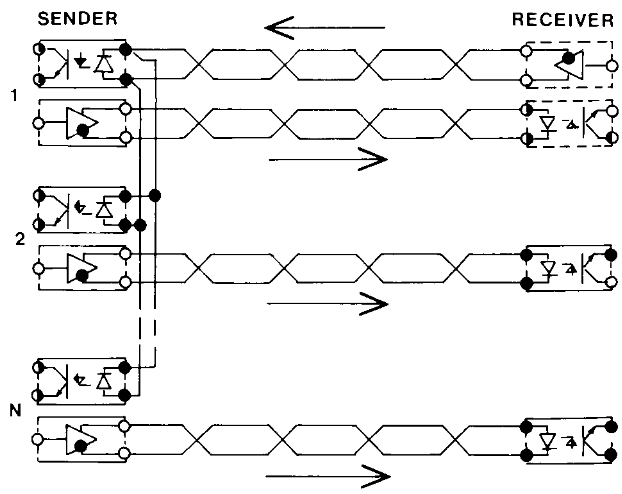
"SSI" ORIGIN

The technological evolution in the 90' which has been applied on numerical controlled machines has generated a request for always more precision of acquirement of the position of the rotating shafts also for high number of turns. This requirement has been satisfied by encoder manufacturers, with an increment of measuring resolution available on single- and multiturn absolute encoders. Industry has got therefore very high precision instruments, fully suitable for the measuring needs but with the inconvenient of the high number of connections to be made for the connection for the encoder to the control system. (Tekel is manufacturing multiturn encoders with resolutions up to 8192 steps per turn x 4096 turns which supply on output 25 signal bit, to which same quantity of integrated conductors with power supply and input and output optional signals must correspond .
In order to reduce the installation costs and in order to simplify the connections the synchronus serial interface , better know as SSI, has been developed and is catching always higher interest from industry.

ADVANTAGES OF "SSI" APPLICATION

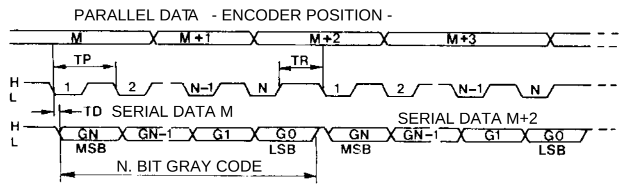
The SSI application has immediately given advantages for the user such as:

- easier wiring with the use of only 6 screened conductors for any possible resolution request
- possibility to update of the resolution of an existing machinery without expensive wiring modifications
- reliability of the code with Gray format
- extreme simplicity and low cost for the conversion of the Gray code into Binary (please refer to page 14)
- possibility to adapt the encoder transmission speed depending from the transmission distance
- further reduction of the connections quantity thanks to the possibility to use only one CLOCK (***2 conducers***) for a group of encoders each of which transmits on his own double wire possibility to determine the time and the transmission speed directly from the ***control board***.

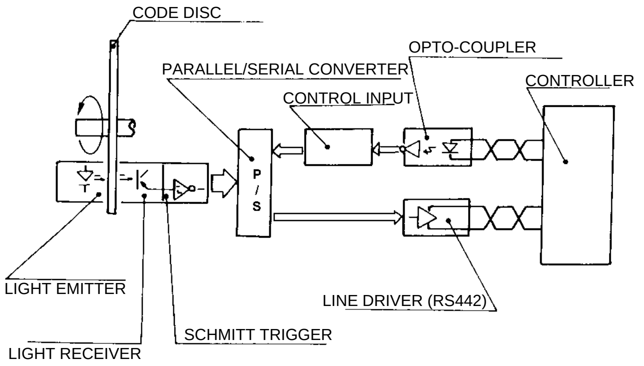


FUNCIONING PRINCIPALS

The optical code reading systems includes one or more coded disks, gives constantly the updated position values. The generated code is presented on the input of a parallel/serial converter (P/S) controlled on synchronus mode by a ckock frequence received on the CKI and CKI inputs)see figure on page 10).
These signals do assume on rest state the logic value "1" or "high", the controller asks the encoder for information on his position by sending a train of clock pulses which number depends from the number of bits which have to be transmitted (encoder resolution) and from the activated transmission protocol. At the first LOW/HIGH transition the code at converter P/S input is loaded; the next "LOW-HIGH" transaction gives on P/S converter output, the MSB code. Each subsequent trains pulse "LOW/HIGH" transaction gives the next bit on the line OUT.
At the end of the pulses sequence established by the protocol used, and after a minimum time corresponding to ½ clock pulse, the output goes back to rest state allowing the continuous update of the data in the P/S converter.



BLOCK DIAGRAM



TECHNICAL CHARACTERISTICS

INPUT CLOCK (CKI, $\overline{\text{CKI}}$)

Input type	complemented signals
Minimal Frequency	100 kHz
Maximal Frequency	1100 kHz
Minimal current @ 1,1 MHz	6,6 mA
Maximal current	20 mA
Line status at rest state (not on transmission)	1 logic (CKI =HIGH, CKI = LOW)

OUTPUT DATA (OUT, $\overline{\text{OUT}}$)

Output signal type	complemented
Transmission levels	compatible with RS422
Line driver type	26LS31
Line status at rest state (not on transmission)	1 logic (OUT = HIGH , OUT = LOW)
Transmitted code type	standard: Gray

CONNECTIONS

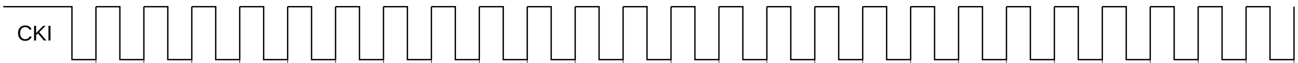
Number of required conducers	4 + 2 supply + ground (not depending from number of resolutions bits)
Connecting cable characteristics	3 twisteed shielded double cable
Allowed transmission distance	25, 50, 100, 200, 400 m
Baud Rate (influences the transmission distance)	800, 400, 300, 200, 100 kHz

TRANSMISSION PROTOCOL

Max number of transmitted bit	26
Max resolution of transmitted data	8192 PPR x 4096 RPM
Supported transmission formats	13, 21, 24, 25, 26 right, left or center justified
Transmission time	Tp = 0,5 ÷ 10 µs (clock frequency function) Td = 1/2 Tp + 2 µs Tr = 12 ÷ 25 µs (clock frequency function)

TRANSMISSION PROTOCOL

MSB LSB



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
4096	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	8192
2048	0	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	4096
1024	0	0	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	2048
512	0	0	0	N9	N8	N7	N6	N5	N4	N3	N2	N1	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	1024
256	0	0	0	0	N8	N7	N6	N5	N4	N3	N2	N1	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	512
128	0	0	0	0	0	N7	N6	N5	N4	N3	N2	N1	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	0	256
64	0	0	0	0	0	0	N6	N5	N4	N3	N2	N1	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	0	0	128
32	0	0	0	0	0	0	0	N5	N4	N3	N2	N1	P6	P5	P4	P3	P2	P1	0	0	0	0	0	0	0	64
16	0	0	0	0	0	0	0	0	N4	N3	N2	N1	P5	P4	P3	P2	P1	0	0	0	0	0	0	0	0	32
8	0	0	0	0	0	0	0	0	0	N3	N2	N1	P4	P3	P2	P1	0	0	0	0	0	0	0	0	0	16
4	0	0	0	0	0	0	0	0	0	0	N2	N1	P3	P2	P1	0	0	0	0	0	0	0	0	0	0	8
2	0	0	0	0	0	0	0	0	0	0	0	N1	P2	P1	0	0	0	0	0	0	0	0	0	0	0	4

Nr. of turns ⇐ ⇒ Steps per turns

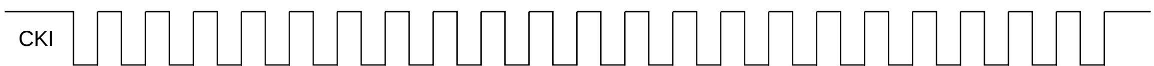
The transmission protocol is determined by 4 characteristic parameters (2 compulsory and 2 optional) as follows:

Transmitted word length
This is the number of bit which compose the pulses train transmitted as clock: this gives the maximal resolution which can be transmitted in only one interrogation. The are 4 available formats: 13,21,24,25 bit. A fifth format with 26 bit foresees a code with 25 bit + final parity on bit 26.

Alignment types
In case the number of general bits, in relation to the resolution per turns and to the number of turns, is lower than the number of protocol defined bit, the word is transmitted by introducing an “offset” which “aligns” the code on a predetermined position in the response pulses train.
The Tekel encoders allow three different alignment options: central (or pine shape) , to the right, to the left; on which the offset is respectively:

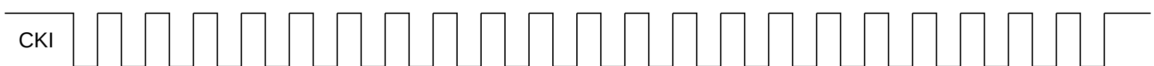
- devided by obtaining 2 parts, which , depending from number of turns and number of steps per turn , are allocated
- ahead and at the end of the code.
- added at the end of the code
- added ahead of the code

LEFT



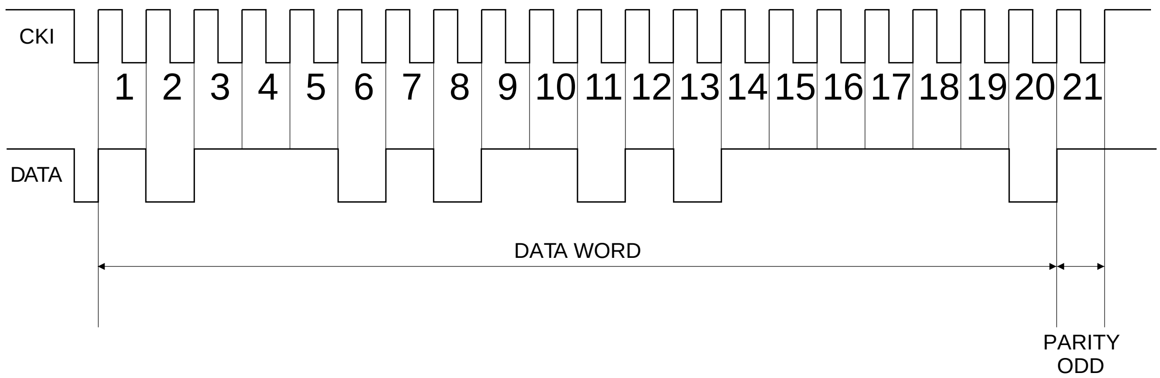
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
512 x 256	G^{16}	G^{15}	G^{14}	G^{13}	G^{12}	G^{11}	G^{10}	G^{9}	G^{8}	G^{7}	G^{6}	G^{5}	G^{4}	G^{3}	G^{2}	G^{1}	G^{0}	0	0	0	0

RIGTH



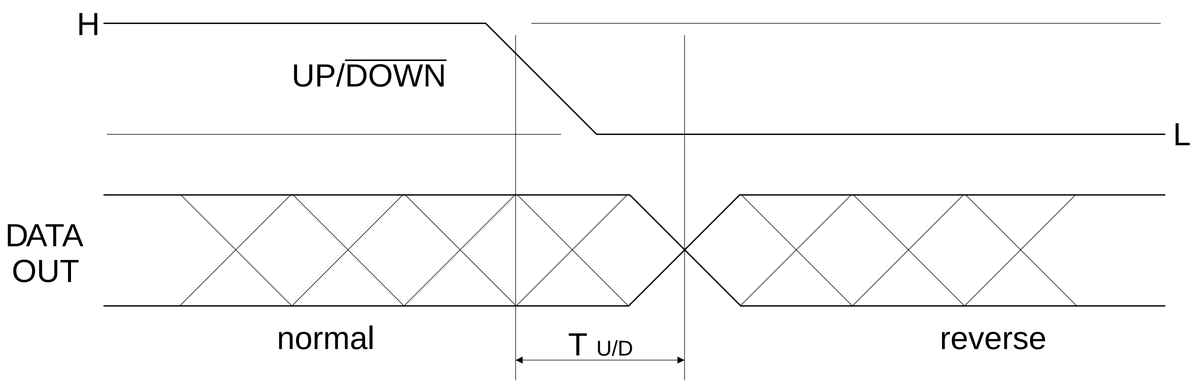
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
512 x 256	0	0	0	0	G^{16}	G^{15}	G^{14}	G^{13}	G^{12}	G^{11}	G^{10}	G^{9}	G^{8}	G^{7}	G^{6}	G^{5}	G^{4}	G^{3}	G^{2}	G^{1}	G^{0}

Parity check (optional)
One of the simplest and most common methods to identify errors in a package of data interchanged between two devices (for example encoder and controls system) consist in introducing 1 adding bit at the end of the code which identifies the parity:
- in case of parity “ODD” (O) this bit has value 1 if the sum of the bit at “1” in the code, excluded the parity bit, is even; the value is “0” in case the number of bit at “1” is odd.
- in case of parity “.EVEN” this bit has value 1 if the sum of the bit at “1” in the code, excluded the parity bit, is odd; the value is “0” in case the number of bit at “1” is even.



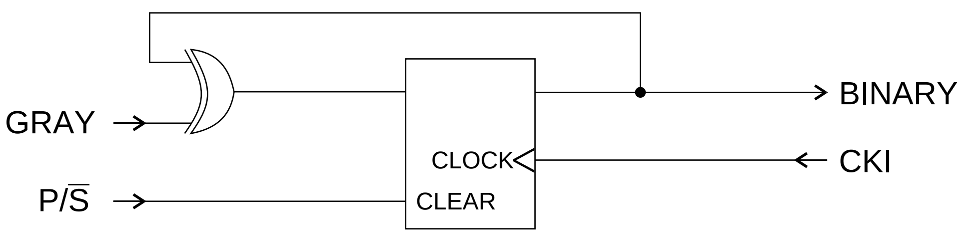
Up/Down (optional)
We remind that the Tekel encoders are designed in order to:
- increment counting when shaft rotates clockwise.
- decrement counting when shaft rotates counter clockwise.

The control of theUp/Down signal allows the invert the functioning logic with consequent decrement of signal when shaft rotates clockwise or vice versa. The activation of input Up/Down has consequence on the transmitted code with a certain delay which is defined TU/D time.



APPLICATION NOTES

Gray Binary conversion
A useful characteristic of serial data transmission, through SSI, consists in the extremely easy conversion of the data from Gray to Binary format. Only 2 components are sufficient: a port EXCLUSIVE-OR and a FLIP-FLOP.



CONNECTIONS - Absolute encoders TKE series

(for BCD code connections please sea TKC models)

TEKEL INSTRUMENTS

MS 26 P CONNECTOR S26 - SL26	D 25 P CONNECTOR D25	CABLE COLOUR	GRAY signals	BINARY signals	LEGENDA: Because of the small space on the label we had to abbreviate cable colours as follows			
A	2	WHT	G^0	2^0	1	WHT	=	white
B	15	PNK	G^1	2^1	6	PNK	=	pink
C	3	BLU	G^2	2^2	7	BLU	=	blue
D	16	YLW	G^3	2^3	4	YLW	=	yellow
E	4	GRN	G^4	2^4	3	GRN	=	green
F	17	BRW	G^5	2^5	2	BRW	=	brown
G	5	GRY	G^6	2^6	5	GRY	=	grey
H	18	VLT	G^7	2^7	10	VLT	=	violet
J	6	WHT/BLK	G^8	2^8	25	WHT/BLK	=	white and black
K	19	WHT/RED	G^9	2^9	23	WHT/RED	=	white and red
R	22	GRY/BRW	ZERO	ZERO	18	GRY/BRW	=	grey and brown
M	13	RED/BLU	MSB*	MSB*	12	RED/BLU	=	red and blue
W	10	WHT/GRN	U/$\overline{D}$	U/$\overline{D}$	13	WHT/GRN	=	white and green
N	14	WHT/YLW	$\overline{MSB}$*	$\overline{MSB}$*	15	WHT/YLW	=	white and yellow
Y	**25**	**RED**	**+ Vcc**	**+ Vcc**	8	RED	=	red
Z	**1**	**BLK**	**0 Volt**	**0 Volt**	9	BLK	=	black

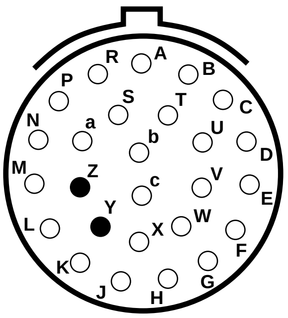
The relative number of the cable colour code meets DIN 47100 requirements.

*** JUMPERS** (to program the up-down counts related to CW or CCW rotation of shaft)
-MSB and U/D for CW rotation counting UP
-MSB and U/D for CCW rotation counting UP

CONNECTOR MS3112A 16-26 otherwise called MS 26 P

ORDER CODE S26 o SL26

PIN	SIGN	PIN	SIGN	PIN	SIGN	PIN	SIGN	PIN	SIGN	PIN	SIGN
A	2^0	E	2^4	J	2^8	N	$\overline{MSB}$*	T	VOID	X	VOID
B	2^1	F	2^5	K	2^9	P	VOID	U	VOID	Y	+ Vcc
C	2^2	G	2^6	L	VOID	R	ZERO	V	VOID	Z	0 Volt
D	2^3	H	2^7	M	MSB*	S	VOID	W	U/$\overline{D}$	a	VOID
b	N.C.	c	N.C.								

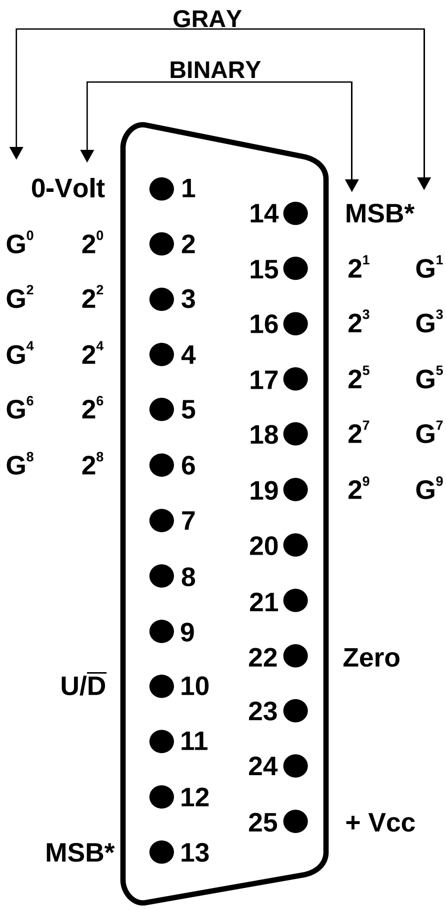


Y = + Vcc

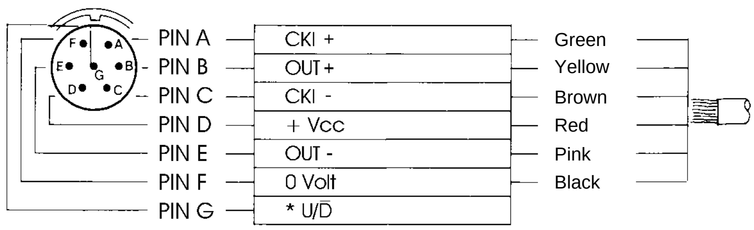
Z = 0 Volt

CONNECTOR D 25P

ORDER CODE D25



CONNECTION DIAGRAM FOR TKE 615 WITH SYNCHROTEK® INTERFACE



* Jumper: pin U/D and 0 Volt for CCW rotation

CKI/CKI INVERTED = INPUT CLOCK LINE
OUT/OUT INVERTED = OUTPUT DATA LINE

CONNECTIONS - Absolute encoders TKC series

CONNECTOR MS 26 PIN DESIGNATION Cod. S26 o SL26	CONNECTOR D 25 PIN DESIGNATION Cod. D25	RIF. DIN 47100	CABLE COLOUR	GRAY Signals	BINARY Signals	GRAY Excess 3* Signals	Signal BCD code
A	2	1	WHT	G^{0}	2^{0}	G^{0}	1.10^{0}
B	15	6	PNK	G^{1}	2^{1}	G^{1}	2.10^{0}
C	3	7	BLU	G^{2}	2^{2}	G^{2}	4.10^{0}
D	16	4	YLW	G^{3}	2^{3}	G^{3}	8.10^{0}
E	4	3	GRN	G^{4}	2^{4}	G^{0}	1.10^{1}
F	17	2	BRW	G^{5}	2^{5}	G^{1}	2.10^{1}
G	5	5	GRY	G^{6}	2^{6}	G^{2}	4.10^{1}
H	18	10	VLT	G^{7}	2^{7}	G^{3}	8.10^{1}
J	6	25	WHT/BLK	G^{8}	2^{8}	G^{0}	1.10^{2}
K	19	23	WHT/RED	G^{9}	2^{9}	G^{1}	2.10^{2}
L	7	21	WHT/BLU	G^{10}	2^{10}	G^{2}	4.10^{2}
M	20	26	BRW/BLK	G^{11}	2^{11}	G^{3}	8.10^{2}
N	8	20	PNK/BRW	G^{12}	2^{12}	G^{0}	1.10^{3}
P	21	19	WHT/PNK	NC	NC	G^{1}	2.10^{3}
R	22	18	GRY/BRW	ZERO	ZERO	ZERO	ZERO
S	11	17	WHT/GRY	PARITY	PARITY	PARITY	PARITY
T	9	24	BRW/RED	NC	NC	G^{2}	4.10^{3}
U	12	22	BRW/BLU	ENABLE	ENABLE	ENABLE	ENABLE
V	23	16	YLW/BRW	VOID	STROBE	VOID	STROBE
W	10	13	WHT/GRN	$U/\overline{D}$*	$U/\overline{D}$*	$U/\overline{D}$*	$U/\overline{D}$*
X	24	14	BRW/GRN	LATCH	LATCH	LATCH	LATCH
Y	**25**	**8**	**RED**	+ Vcc	+ Vcc	+ Vcc	+ Vcc
Z	**1**	**9**	**BLK**	0 Volt	0 Volt	0 Volt	0 Volt
a	13	11	GRY/PNK	NC	NC	G^{3}	8.10^{3}
b	14	15	WHT/YLW	ZERO SET	ZERO SET	ZERO SET	ZERO SET
c	--	12	RED/BLU	VOID	VOID	VOID	VOID

***** CW SHAFT ROTATION and LEVEL "1" = count UP
CW SHAFT ROTATION and LEVEL "0" = count DOWN and vice versa

LEGEND
Due to the lack of space on the label cable colours where abbreviated as follows:

1 WHT = white
6 PNK = pink
7 BLU = blue
4 YLW = yellow
3 GRN = green
2 BRW = brown
5 GRY = grey
10 VLT = violet
8 RED = red
9 BLK = black

25 WHT/BLK = white and black
23 WHT/RED = white and red
21 WHT/BLU = white and blue
26 BRW/BLK = brown and black
20 PNK/BRW = pink and brown
19 WHT/PNK = white and pink
18 GRY/BRW = grey and brown
17 WHT/GRY = white and grey
24 BRW/RED = brown and red
22 BRW/BLU = brown and blue

16 YLW/BRW = yellow and brown
13 WHT/GRN = white and green
14 BRW/GRN = brown and green
11 GRY/PNK = grey and pink
15 WHT/YLW = white and yellow
12 RED/BLU = red and blue

The relative number of the cable colour code meets DIN 47100 requirements.

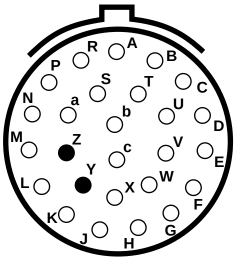
CONNECTIONS - Absolute encoders TKC series

CONNECTOR MS3112A 16-26P otherwise called MS 26P

ORDER CODE S26 o SL26

GRAY AND BINARY		GRAY EXCESS 3 and BCD	
PIN	SIGNAL	PIN	SIGNAL
A	$G^0/2^0$	A	$G^0/1.10^0$
B	$G^1/2^1$	B	$G^1/2.10^0$
C	$G^2/2^2$	C	$G^2/4.10^0$
D	$G^3/2^3$	D	$G^3/8.10^0$
E	$G^4/2^4$	E	$G^0/1.10^1$
F	$G^5/2^5$	F	$G^1/2.10^1$
G	$G^6/2^6$	G	$G^2/4.10^1$
H	$G^7/2^7$	H	$G^3/8.10^1$
J	$G^8/2^8$	J	$G^0/1.10^2$
K	$G^9/2^9$	K	$G^1/2.10^2$
L	$G^{10}/2^{10}$	L	$G^2/4.10^2$
M	$G^{11}/2^{11}$	M	$G^3/8.10^2$
N	$G^{12}/2^{12}$	N	$G^0/1.10^3$
P	N.C.	P	$G^1/2.10^3$
R	ZERO SIGNAL	R	ZERO SIGNAL
S	PARITY	S	PARITY
T	VOID	T	$G^2/4.10^3$
U	$\overline{\text{ENABLE}}$ (3-STATE)	U	$\overline{\text{ENABLE}}$ (3-STATE)
V	STROBE	V	STROBE
W	U/$\overline{\text{D}}$	W	U/$\overline{\text{D}}$
X	$\overline{\text{LATCH}}$	X	$\overline{\text{LATCH}}$
Y	+ Vcc	Y	+ Vcc
Z	0 Volt	Z	0 Volt
a	VOID	a	VOID
b	VOID	b	VOID
c	VOID	c	VOID

S26 o SL26

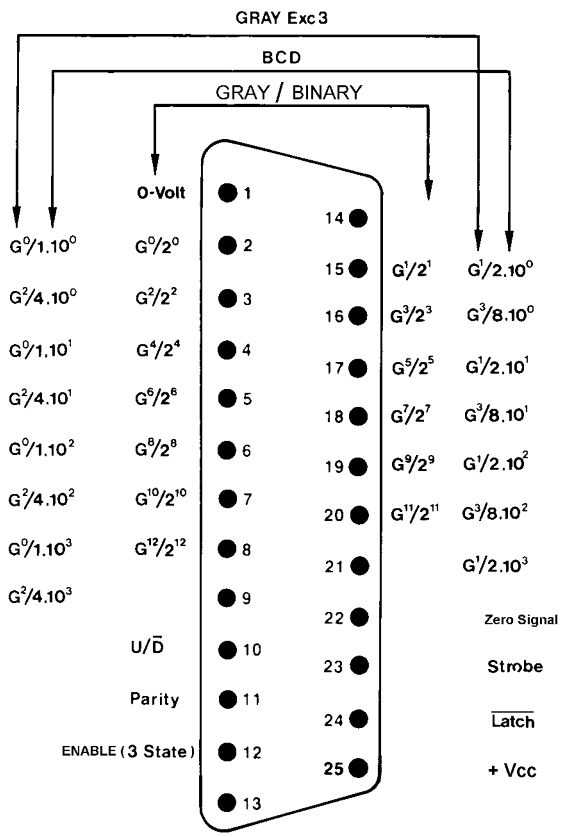


Y = + Vcc

Z = 0 Volt

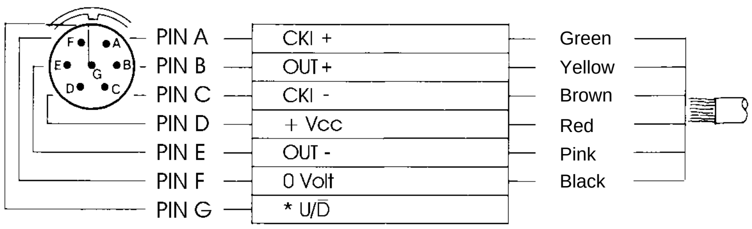
CONNECTOR D 25 P

ORDER CODE D25



CONNECTION DIAGRAM FOR SSI INTERFACE

7 pins connector MS3106A 16A 16S-1P



* For CCW rotation: Jump pin U/D and 0 Volt

CKI/CKI INVERTED = INPUT CLOCK LINE
OUT/OUT INVERTED= OUTPUT CLOCK LINE

For TKM60P (programmable version)

12 pins connector - Ordering code S12 o SL12

Connections for 12 pins connector

Metal connector shield on housing

PIN	SIGNAL
1	0 Volt
2	Data +
3	CKI +
4	Rx +
5	Rx -
6	Tx +
7	Tx -
8	+ Vcc
9	Zero set
10	Data -
11	CKI -
12	Up/$\overline{\text{Down}}$

Pins 4–7: RS 432 RS 485 programming serial interface.
For RS 232 connect only Tx+ and Rx+

For TKC - TKM (not programmable versions)

12 pin connector - Ordering code S12 o SL12

Connections for 12 pins connector

Metal connector shield on housing

PIN	SIGNAL
1	0 Volt
2	Data +
3	CKI +
4	n.c.
5	n.c.
6	n.c.
7	n.c.
8	+ Vcc
9	Zero set
10	Data -
11	CKI -
12	Up/$\overline{\text{Down}}$

Connector 17 pin (Conin)

Ordering code S17 o SL17

PIN	9 bit	10 bit	12 bit	13 bit
1	D0 (LSB)	D0 (LSB)	D0 (LSB)	D0 (LSB)
2	D1	D1	D1	D1
3	D2	D2	D2	D2
4	D3	D3	D3	D3
5	D4	D4	D4	D4
6	D5	D5	D5	D5
7	D6	D6	D6	D6
8	D7	D7	D7	D7
9	D8 (MSB)	D8	D8	D8
10	n.c.	D9 (MSB)	D9	D9
11	n.c.	n.c.	D10	D10
12	$\overline{\text{Enable}}$	$\overline{\text{Enable}}$	D11 (MSB)	D11
13	Strobe/$\overline{\text{Latch}}$*	Strobe/$\overline{\text{Latch}}$*	Strobe/$\overline{\text{Latch}}$*	Strobe/$\overline{\text{Latch}}$*
14	U/$\overline{\text{D}}$	U/$\overline{\text{D}}$	U/$\overline{\text{D}}$	U/$\overline{\text{D}}$
15	0 Volt	0 Volt	0 Volt	0 Volt
16	+ Vcc	+ Vcc	+ Vcc	+ Vcc
17	$\overline{\text{Alarm}}$	$\overline{\text{Alarm}}$	$\overline{\text{Alarm}}$	D12 (MSB)

(*) Supplied normally $\overline{\text{STROBE}}$ is on request (option L/P) $\overline{\text{LATCH}}$.

TKM CONNECTIONS

DESIGNATION CONNECTION Cod. S26 o SL26 S32 o SL32		DESIGNATION CONNECTION Cod. D25 o D37		CABLE COLOUR Cod. P - PL	Cod. P - PL	GRAY CODE SIGNALS	BINARY CODE SIGNALS	GRAY EXC.3 CODE SIGNALS	BCD CODE SIGNALS
MS 26P	**MS 32P**	**D 25**	**D 37***	**26 wires**	**37 wires**				
A	A	2	2	WHT	WHT	G^{0}	2^{0}	G^{0}	1.10^{0}
B	B	15	21	PNK	PNK	G^{1}	2^{1}	G^{1}	2.10^{0}
C	C	3	3	BLU	BLU	G^{2}	2^{2}	G^{2}	4.10^{0}
D	D	16	22	YLW	YLW	G^{3}	2^{3}	G^{3}	8.10^{0}
E	E	4	4	GRN	GRN	G^{4}	2^{4}	G^{0}	1.10^{1}
F	F	17	23	BRW	BRW	G^{5}	2^{5}	G^{1}	2.10^{1}
G	G	5	5	GRY	GRY	G^{6}	2^{6}	G^{2}	4.10^{1}
H	H	18	24	VLT	VLT	G^{7}	2^{7}	G^{3}	8.10^{1}
J	J	6	6	WHT/BLK	WHT/BLK	G^{8}	2^{8}	G^{0}	1.10^{2}
K	K	19	25	WHT/RED	WHT/RED	G^{9}	2^{9}	G^{1}	2.10^{2}
L	L	7	7	WHT/BLU	WHT/BLU	G^{10}	2^{10}	G^{2}	4.10^{2}
M	M	20	26	BRW/BLK	BRW/BLK	G^{11}	2^{11}	G^{3}	8.10^{2}
N	N	8	8	PNK/BRW	BRW/PNK	G^{12}	2^{12}	G^{0}	1.10^{3}
P	P	21	27	WHT/PNK	WHT/PNK	G^{13}	2^{13}	G^{1}	2.10^{3}
R	R	23	29	WHT/YLT	GRN/BLK	$\overline{\text{ZERO SET}}$	$\overline{\text{ZERO SET}}$	$\overline{\text{ZERO SET}}$	$\overline{\text{ZERO SET}}$
S	S	11	11	WHT/GRY	WHT/GRY	PARITY (TX)	PARITY	PARITY	PARITY
T	T	9	9	BRW/RED	BRW/RED	G^{14}	2^{14}	G^{2}	4.10^{3}
U	U	12	12	BRW/BLU	BRW/BLU	ENABLE (RX)	ENABLE	ENABLE	ENABLE
V	V	25	32	BRW/YLW	YLW/BRW	-	STROBE	-	STROBE
W	W	10	10	WHT/GRN	WHT/GRN	$U/\overline{D}$**	$U/\overline{D}$**	$U/\overline{D}$**	$U/\overline{D}$**
X	X	24	30	BRW/GRN	BRW/GRN	LATCH	LATCH	LATCH	LATCH
Y	**Y**	**13**	**13**	**RED**	**RED**	**+ Vcc**	**+ Vcc**	**+ Vcc**	**+ Vcc**
Z	**Z**	**1**	**1**	**BLK**	**BLK**	**0 Volt**	**0 Volt**	**0 Volt**	**0 Volt**
a	a	22	28	GRY/PNK	YLW/PNK	G^{15}	2^{15}	G^{3}	8.10^{3}
b	b	-	14	GRY/BRW	WHT/YLW	G^{16}	2^{16}	G^{0}	1.10^{14}
c	c	-	33	RED/BLU	YLW/BLU	G^{17}	2^{17}	G^{1}	2.10^{4}
-	d	-	15	-	GRY/BLU	G^{18}	2^{18}	G^{2}	4.10^{4}
-	e	-	34	-	YLW/GRY	G^{19}	2^{19}	G^{3}	8.10^{4}
-	f	-	16	-	GRY/PNK	G^{20}	2^{20}	G^{0}	1.10^{5}
-	g	-	35	-	GRN/RED	G^{21}	2^{21}	G^{1}	2.10^{5}
-	h	-	17	-	PNK/GRN	G^{22}	2^{22}	G^{2}	4.10^{5}
-	j	-	36	-	GRN/BLU	G^{23}	2^{23}	G^{3}	8.10^{5}
-	-	-	18	-	RED/BLU	G^{24}	2^{24}	G^{0}	1.10^{6}
-	-	-	37	-	GRY/BRW	-	-	G^{1}	2.10^{6}
-	-	-	-	-	YLW/RED	-	-	-	-
-	-	-	-	-	YLW/BLK	-	-	-	-
-	-	-	-	-	GRY/GRN	-	-	-	-

* only TKM 100
** CW SHAFT ROTATION and LEVEL “1” = count UP
CW SHAFT ROTATION and LEVEL “0” count DOWN and vice versa

LEGENDA
Due to the lack of available space on the label the cable colours were abbreviated as follows:

1 WHT = white
6 PNK = pink
7 BLU = blue
4 YLW = yellow
3 GRN = green
2 BRW = brown
5 GRY = grey
10 VLT = violet
8 RED = red
9 BLK = black

25 WHT/BLK = white and black
23 WHT/RED = white and red
21 WHT/BLU = white and blue
26 BRW/BLK = brown and black
34 YLW/RED = yellow and red
36 YLW/BLK = yellow and black
17 WHT/GRY = white and grey
24 BRW/RED = brown and red
22 BRW/BLU = brown and blue
16 YLW/BRW = yellow and brown

13 WHT/GRN = white and green
14 BRW/GRN = brown and green
27 GRY/GRN = grey and green
15 WHT/YLW = white and yellow
20 PNK/BRW = pink and brown
19 WHT/PNK = white and pink
35 GRN/BLK = green and black
30 YLW/PNK = yellow and pink
32 YLW/BLU = yellow and blue
37 GRY/BLU = grey and blue

28 YLW/GRY =yellow and grey
11 GRY/PNK =grey and pink
33 GRN/RED =green and red
29 PNK/GRN =pink and green
31 GRN/BLU =green and blue
12 RED/BLU =red and blue
18 GRY/BRW =grey and brown

The relative number of the cable colour code meets DIN 47100 requirements.

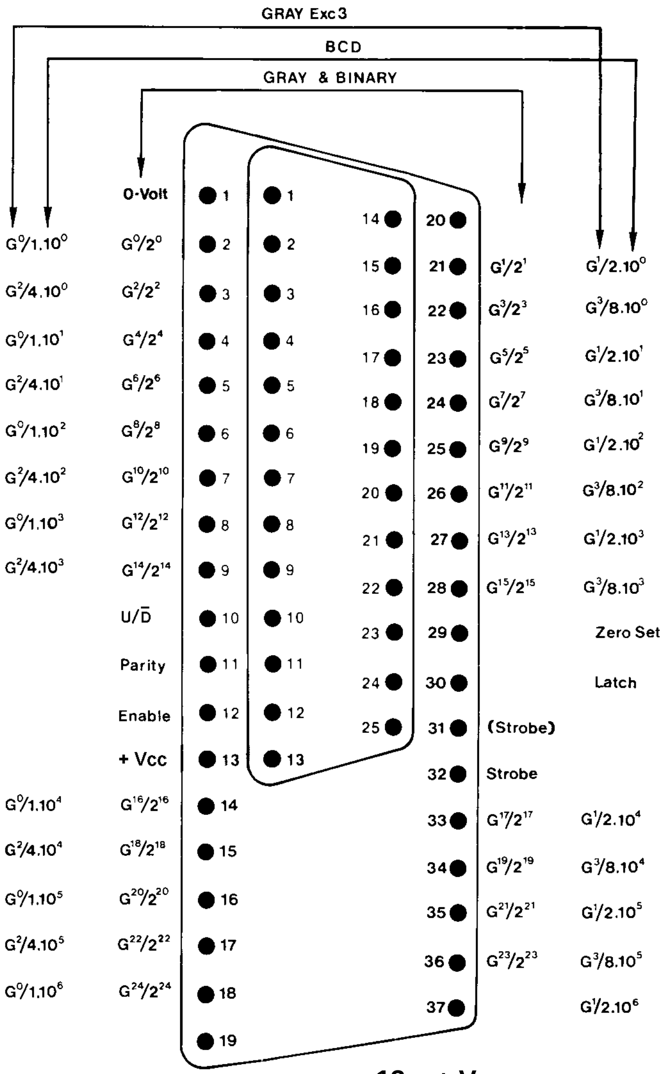
CONNECTIONS - Absolute encoders TKC series

TEKEL INSTRUMENTS

MS3112A 16-26P connector - order code S26 - SI26 MS3112A 18-32P connector - order code S32 - SI32	D25 P connector - order code D25 D37 P connector - order code D37 (*)

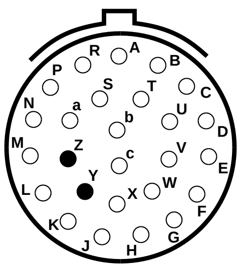
GRAY BINARY | GRAY EXCESS 3 BCD

PIN	SIGNAL	PIN	SIGNAL
A	$G^0/2^0$	A	$G^0/1.10^0$
B	$G^1/2^1$	B	$G^1/2.10^0$
C	$G^2/2^2$	C	$G^2/4.10^0$
D	$G^3/2^3$	D	$G^3/8.10^0$
E	$G^4/2^4$	E	$G^0/1.10^1$
F	$G^5/2^5$	F	$G^1/2.10^1$
G	$G^6/2^6$	G	$G^2/4.10^1$
H	$G^7/2^7$	H	$G^3/8.10^1$
J	$G^8/2^8$	J	$G^0/1.10^2$
K	$G^9/2^9$	K	$G^1/2.10^2$
L	$G^{10}/2^{10}$	L	$G^2/4.10^2$
M	$G^{11}/2^{11}$	M	$G^3/8.10^2$
N	$G^{12}/2^{12}$	N	$G^0/1.10^3$
P	$G^{13}/2^{13}$	P	$G^1/2.10^3$
R	ZERO SET	R	ZERO SET
S	PARITY	S	PARITY
T	$G^{14}/2^{14}$	T	$G^2/4.10^3$
U	ENABLE	U	ENABLE
V	STROBE	V	STROBE
W	U/D̄	W	U/D̄
X	LATCH	X	LATCH
Y	+ Vcc	Y	+ Vcc
Z	0 Volt	Z	0 Volt
a	$G^{15}/2^{15}$	a	$G^3/8.10^3$
b	$G^{16}/2^{16}$	b	$G^0/1.10^4$
c	$G^{17}/2^{17}$ S26-SL26 limit	c	$G^1/2.10^4$
d	$G^{18}/2^{18}$	d	$G^2/4.10^4$
e	$G^{19}/2^{19}$	e	$G^3/8.10^4$
f	$G^{20}/2^{20}$	f	$G^0/1.10^5$
g	$G^{21}/2^{21}$	g	$G^1/2.10^5$
h	$G^{22}/2^{22}$	h	$G^2/4.10^5$
j	$G^{23}/2^{23}$	j	$G^3/8.10^5$

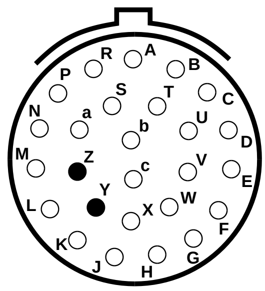


13 = + Vcc
1 = + 0 Volt

S26-SL26



S32-SL32



Y = + Vcc Z = 0 Volt

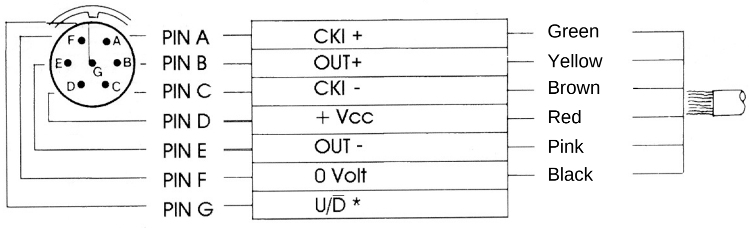
(*) Only for TKM100

Issue 09/1999

CONNECTION SSI INTERFACE

Order code S07-SL07

Output on 7 pin connector MS3102A 16S-1P



* Option available only with output on connector.

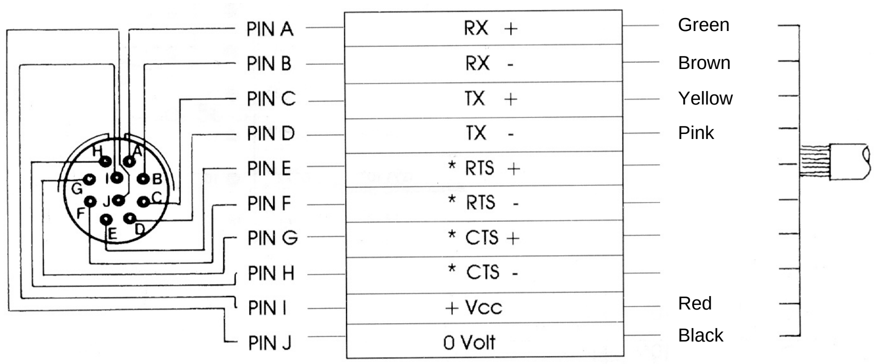
For CCW rotation jump pin U/D and 0Volt

CKI/CKI = INCOMING CLOCK LINE
OUT/OUT = OUTCOMING DATA LINE

Connections RS 232/422/485 SERIAL INTERFECES

Order code S10-SL10

Output on 10 pin connector MS3102A 18S-1P



* Option available only with output on connector.

NPN OUTPUT (NEGATIVE LOGIC)

Fig. 19

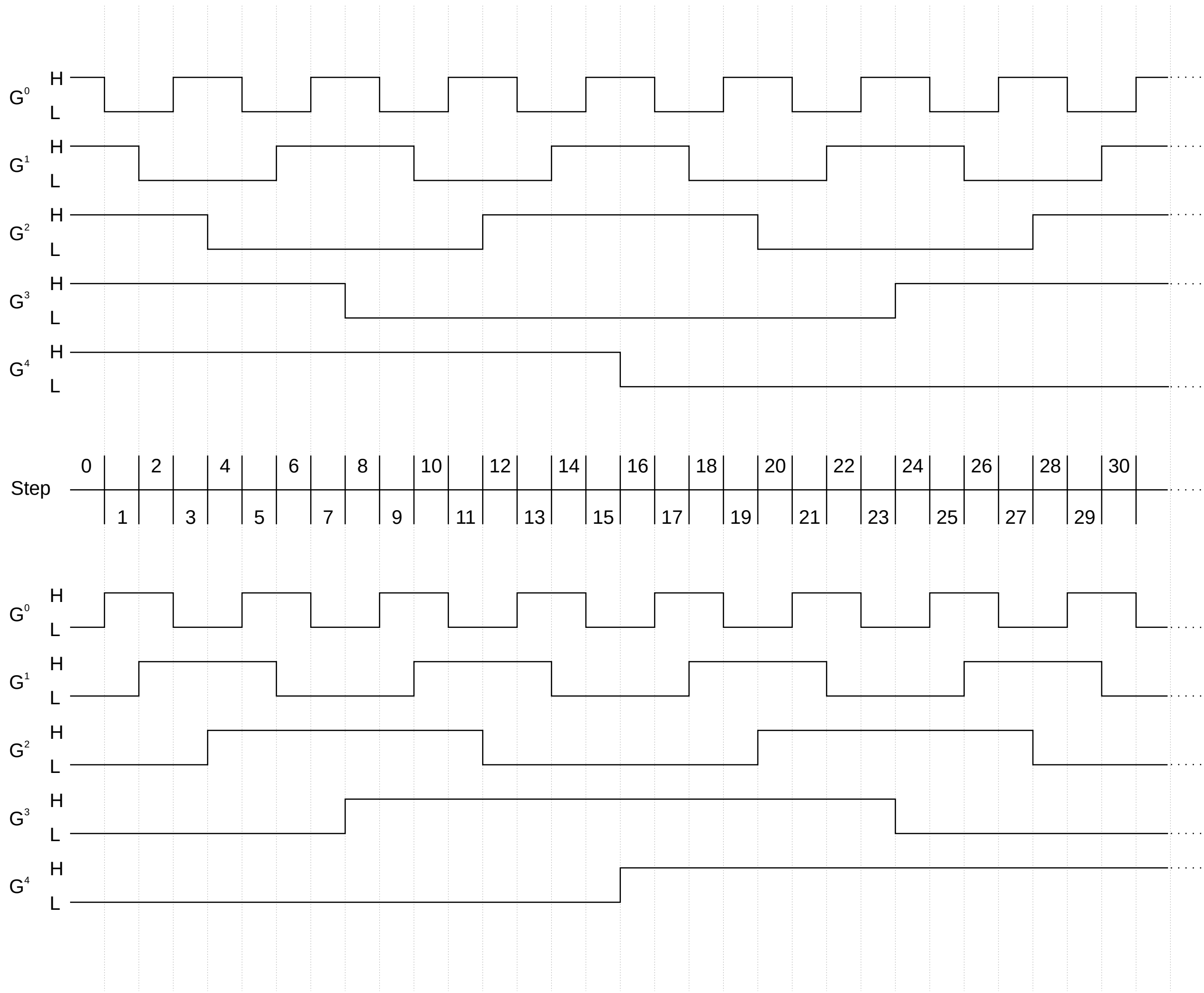


Fig. 20

PNP OUTPUT (POSITIVE LOGIC)

UP/DOWN SELECTION (U/D)
Operating characteristics of up/down - input signal

CW SHAFT ROTATION (Figs. 19 and 20)
Standard version: if the signal is "HIGH" on U/D pin, the code counts "UP";
if the signal is "LOW" on U/D pin, the code counts "DOWN".

CCW SHAFT ROTATION (Figs. 19 and 20)
Standard version: if the signal is "HIGH" on U/D pin, the code counts "DOWN";
if the signal is "LOW" on U/D pin, the code counts "UP".

If the inverted U/D active signal is desired, it is possible, on demand, to change the encoder program.

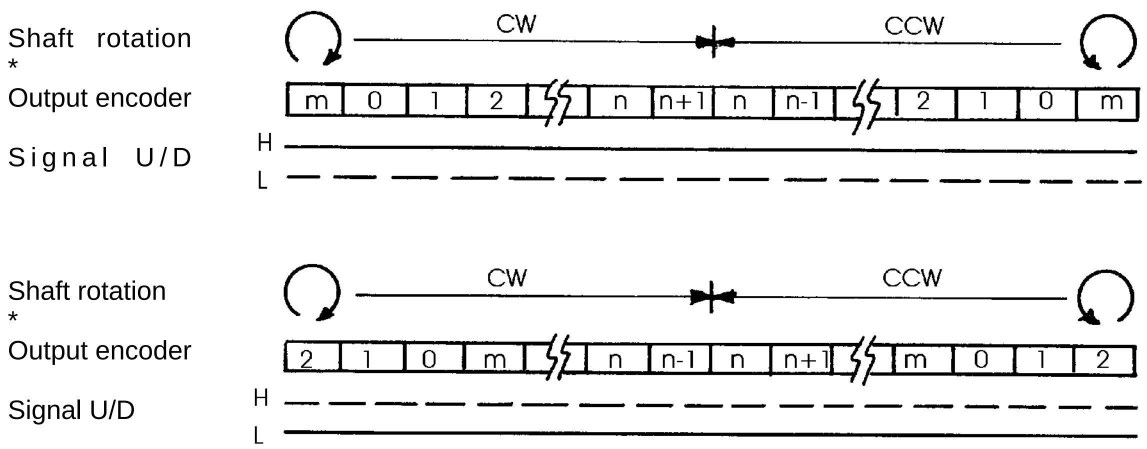


Fig. 21

*Shaft rotation as viewed from front shaft encoder

AVAILABLE FUNCTIONS

LATCH (STORE) FUNCTION

The encoder with this option is equipped with a storage register interposed before the output stage. When a "LOW" signal is addressed to pin "LATCH" the stored information present remains stable until as the same signal "LATCH" goes to "HIGH" level.
The "LATCH" ("STORE") function allows the reading of the encoder in rotation without the risk of information changing during reading time. As shown in Fig. 13 and Fig. 14 the change-over during the transition ("LOW-HIGH") of the signal "STROBE" is used to update the "LATCH" register and this change-over may be used to address the command "STORE" (it must be at "LOW" level) on the "LATCH" pin.

SIGNAL STROBE (dynamic)

The strobe output is a signal generated by the change of the output code and it indicates that the new information is at a stable level.
The standard "STROBE" signal is "HIGH" when the code is ready and "LOW" when the code is switching over (Fig. 13).
The "STROBE" signal can be inverted on demand. (Ordering code: "I").
(*) Sometimes identified with STORE

LATCH, DYNAMIC STROBE

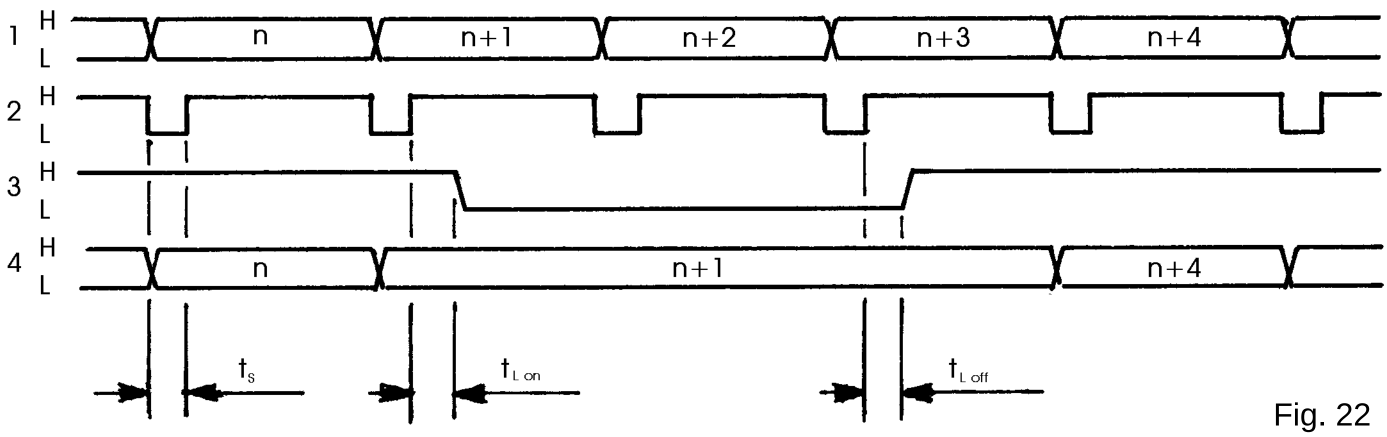


Fig. 22

1=ENCODER; 2=STROBE; 3=$\overline{\text{LATCH}}$; 4=OUTPUT

Switching characteristics

t_s (DYNAMIC STROBE) = 20 microsec. Typical standard (other values on demand).

$t_{L\ on}$ (LATCH ON) > 1 µs
$t_{L\ off}$ (LATCH OFF) > 1 µs

Electrical characteristics

LATCH INPUT (STORE ENABLE)

$V_{I\ HIGH}$ = Vcc related to the chosen voltage
$V_{I\ LOW} \leq 0{,}7$ V
$I_{I\ HIGH} \geq 7$ mA

STROBE OUTPUT

As per interface characteristics NPN, PNP, PUSH-PULL, TTL 3-STATE

AVAILABLE ELECTRONICS

NPN
PNP
PUSH-PULL
TTL 3-STATE
(See LATCH option code 50…80 for TKC series, or option "L" for TKM

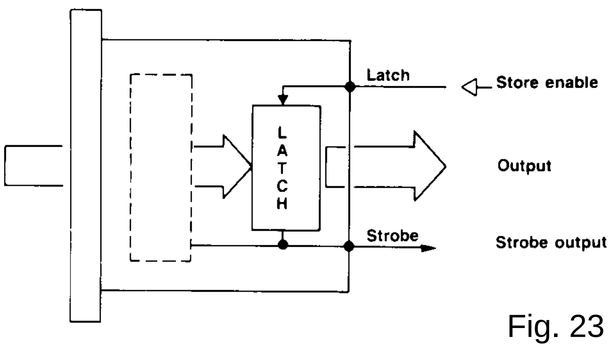


Fig. 23

N.B. The use of LATCH and/or STROBE is necessary with outputs with Binary (B) and BCD (D) code, since otherways it is possible to have reading errors due to measuring system synchronism on the commutation front.

Issue 09/1999

PARITY SIGNAL (electronic)

The “PARITY” is a control signal used for the reading interface and it is used to verify that the information does not contain errors.
The signal “PARITY” is “HIGH” when the Bits that make up the code, in encoder output, are even (Fig.15).
A failure of the interface generates an error.
PARITY output can be:

EVEN, standard version, code “E”
ODD, optional version, code “O”

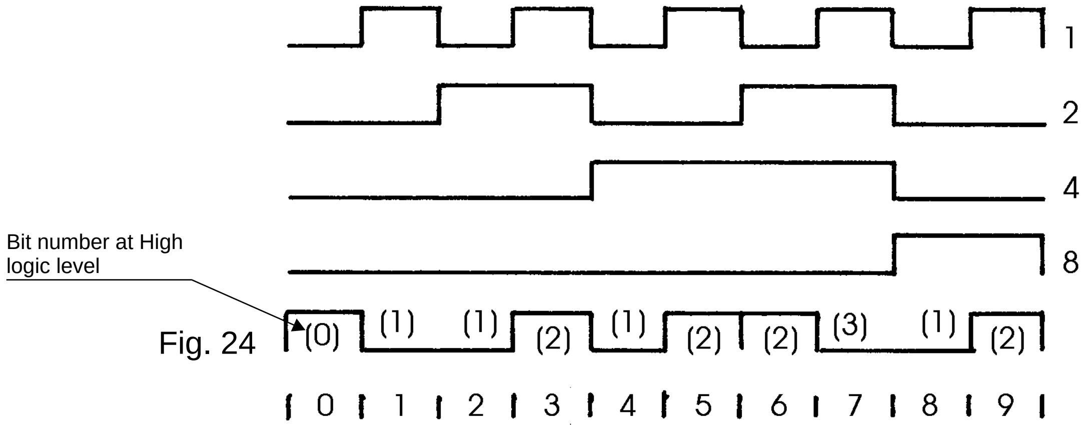


Fig. 24 Odd parity

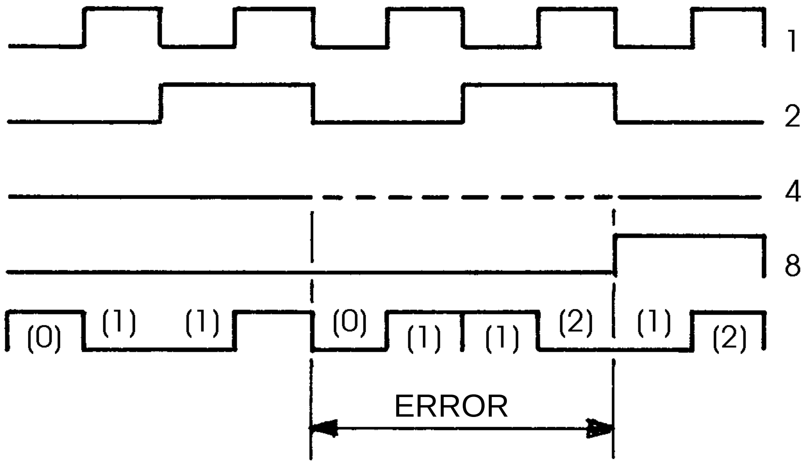


Fig. 25 Odd parity

ZERO SIGNAL
ZERO SIGNAL ordering code “Z”
ZERO SIGNAL DISPLAYED (optional) ordering code “V”
ZERO SIGNAL INTERMEDIATE ordering code “ZI”

The signal “ZERO” is “HIGH” when the code outputs reach the Zero configuration regardless of the chosen code: GRAY, BINARY, BCD or any other (Fig. 17).
When the signal “ZERO” is reached, the LED is “ON” (lighted).
On demand it is possible to program the “ZERO” in an intermediate position with plus-minus counts.
The option “ZERO INTERMEDIATE” is available with a plus-minus “HIGH” signal with or without LED display (Fig. 18).*

*The option “ZERO INTERMEDIATE” (ordering code “ZI”) is available only in CUSTOM version. The angular position must be specified when ordering.

The option “ZERO INTERMEDIATE” is not available with resolutions in code BCD: 1440 2000 2048.

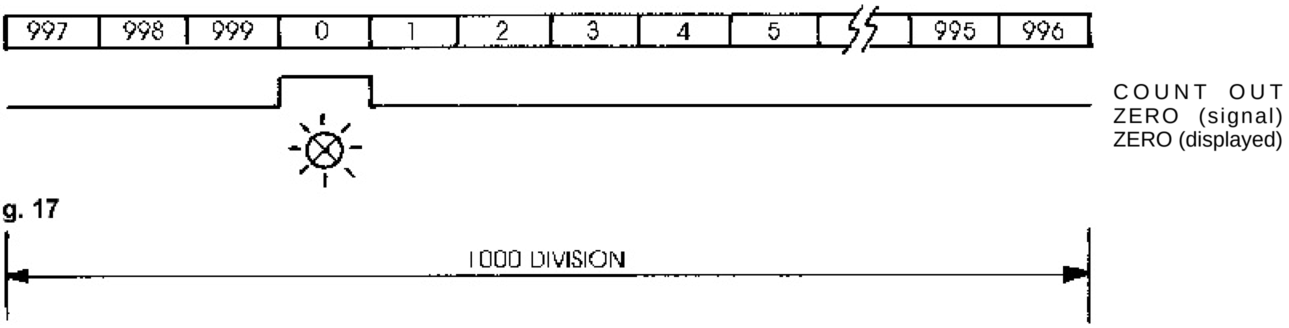


Fig. 17

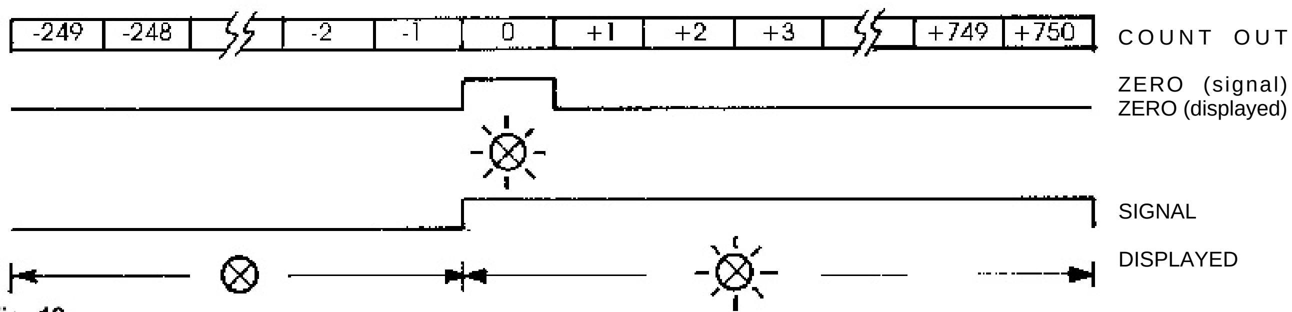
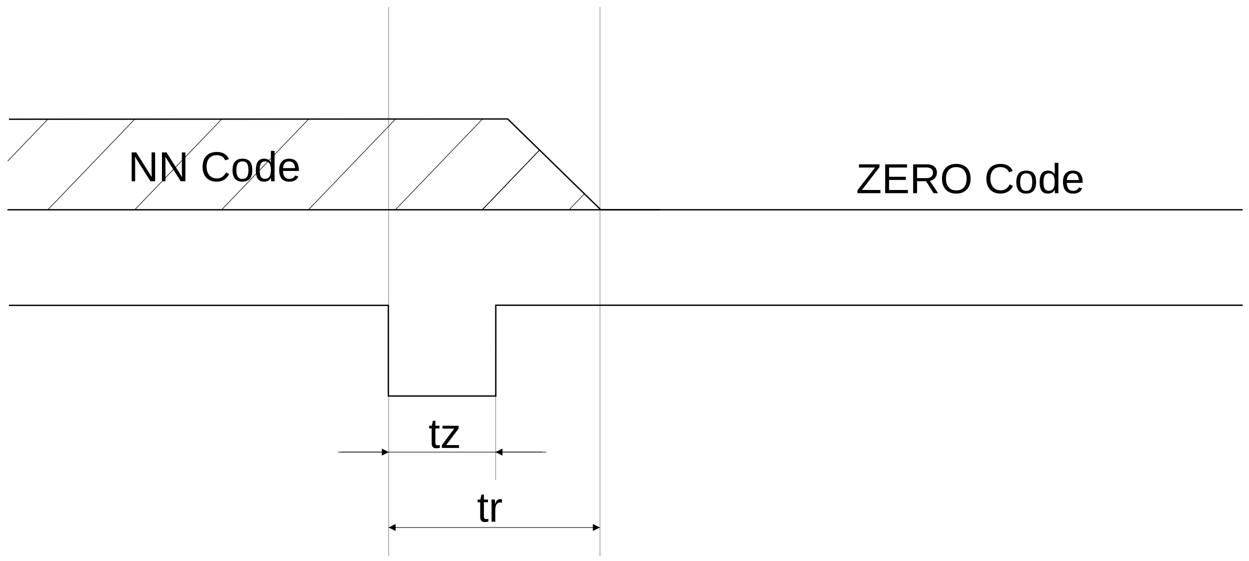


Fig. 18

During the setting of the machinery it may be necessary to set the "zero machine" with the "zero encoder". This operation can be carried out in two ways:
a) turning the shaft of the encoder until the zero signal is found;
b) using the "AUTOMATIC ZERO" option.

NORMAL COUNTING
When the multi-turn encoder is equipped with "AUTOMATIC ZERO" option, in normal counting conditions it is necessary that a voltage +Vdc is present on the pin or on the wire used for this option (for example, if the operative voltage is +5Vdc, the voltage present on the pin or on the wire used for the "AUTOMATIC ZERO" option must be +5Vdc, if the operative voltage is 11-30Vdc, the voltage must range between11-30Vdc). The current available must be 7 mA minimum, 15 mA maximum.

ZERO SETTING PROCEDURE
During the normal counting condition it may be necessary to set the zero machine. In this case the encoder may be in any counting position (for example 16780).
In order to obtain the automatic zero setting of the encoder counting this procedure must be followed:
- convert the voltage of the pin or of the wire used for the "AUTOMATIC ZERO" option from +Vdc to 0 Volt. This condition must remained unchanged for at least 1mSec.
- reconvert the voltage from 0 Volt to +Vdc. Automatically the previous counting position (for example 16780) becomes zero.



tz ⩾ 1 ms
tr = depends from encoder model and code type